## Workshop at a Glance

### Day 1
18 September

**Check-in / Setup:** 0730  
**Welcome:** 0830

**Keynote Addresses**

**Opening Remarks**

**Sessions:**
- **Session 1:** Multicore Technologies
- **Session 2:** Runtime Optimization
- **Focus 2:** US ONLY

(Session 2 and Focus 2 run in parallel)

**Adjourn:** 1700  
1800 Reception  
1845 Banquet Speaker  
1930 Banquet

### Day 2
19 September

**Check-in / Setup:** 0730  
**Announcements:** 0830

**Sessions:**
- **Session 3:** Multicore Hardware Challenges
- **Focus 3:** Cell

(Session 3 and Focus 3 run in parallel)

- **Poster / Demo B:** FPGA Technologies and Applications
- **Session 4:** Novel Applications
- **Focus 4:** GPUs

(Session 4 and Focus 4 run in parallel)

**Panel:** Multicore Meltdown?

**Adjourn:** 1715

### Day 3
20 September

**Check-in / Setup:** 0730  
**Announcements:** 0830

**Sessions:**
- **Session 5:** Multicore Environments
- **Focus 5:** Benchmarking

(Session 5 and Focus 5 run in parallel)

- **Poster / Demo C:** Cell / GPU Technologies
- **Session 6:** Awards Session

**Adjourn:** 1730
### AGENDA

**18 September**

#### Day 1 at a Glance

<table>
<thead>
<tr>
<th>Time</th>
<th>Event</th>
<th>Location</th>
</tr>
</thead>
<tbody>
<tr>
<td>0730</td>
<td>Check-in / Poster Setup / Continental Breakfast</td>
<td></td>
</tr>
<tr>
<td>0830</td>
<td>Welcome: Mr. David Martinez / MIT Lincoln Laboratory</td>
<td></td>
</tr>
<tr>
<td>0835</td>
<td><strong>Mission Keynote Speaker:</strong> Dr. Michael McGrath / DASN (RDT &amp; E)</td>
<td></td>
</tr>
<tr>
<td>0905</td>
<td><strong>Technology Keynote Speaker:</strong> Prof. Jack Dongarra / University of Tennessee, ICL</td>
<td></td>
</tr>
<tr>
<td>0935</td>
<td>Opening Remarks: Mr. Robert Bond / MIT Lincoln Laboratory</td>
<td></td>
</tr>
<tr>
<td>0940</td>
<td><strong>Session 1: Multicore Technologies</strong></td>
<td>Auditorium</td>
</tr>
<tr>
<td>0945</td>
<td>Invited Speaker: Saman Amarasinghe / Massachusetts Institute of Technology CSAIL</td>
<td></td>
</tr>
<tr>
<td>1015</td>
<td>Break</td>
<td>Room S2-180</td>
</tr>
<tr>
<td>1030</td>
<td>Kenneth Prager / Raytheon Company</td>
<td></td>
</tr>
<tr>
<td>1100</td>
<td>Invited Speaker: Hans Zima / Jet Propulsion Laboratory, California Institute of Technology; Institute of Scientific Computing, University of Vienna, Austria</td>
<td></td>
</tr>
<tr>
<td>1130</td>
<td>Poster / Demo A: Advanced Algorithms and Hardware</td>
<td></td>
</tr>
<tr>
<td>1225</td>
<td>Lunch (View Posters)</td>
<td></td>
</tr>
<tr>
<td>1345</td>
<td><strong>Session 2: Runtime Optimization</strong></td>
<td>1345 Focus 2: US ONLY</td>
</tr>
<tr>
<td>1355</td>
<td>Albert Reuther / MIT Lincoln Laboratory</td>
<td></td>
</tr>
<tr>
<td>1425</td>
<td>Daniel Waddington / Lockheed Martin Corporation</td>
<td></td>
</tr>
<tr>
<td>1455</td>
<td>Dong-In Kang / University of Southern California, ISI</td>
<td></td>
</tr>
<tr>
<td>1525</td>
<td>Break (View Posters)</td>
<td></td>
</tr>
<tr>
<td>1550</td>
<td>Invited Speaker: David Scott / Intel Corporation</td>
<td></td>
</tr>
<tr>
<td>1620</td>
<td>Invited Speaker: Zachary Lemnios / MIT Lincoln Laboratory</td>
<td></td>
</tr>
<tr>
<td>1650</td>
<td><strong>Closing Remarks:</strong> Jeremy Kepner / MIT Lincoln Laboratory</td>
<td></td>
</tr>
<tr>
<td>1700</td>
<td>Adjoin</td>
<td></td>
</tr>
<tr>
<td>1800</td>
<td>Reception</td>
<td></td>
</tr>
<tr>
<td>1845</td>
<td><strong>Banquet Speaker:</strong> Mr. Doug Malewicki / AeroVisions, Inc.</td>
<td></td>
</tr>
<tr>
<td>1930</td>
<td>Banquet</td>
<td></td>
</tr>
</tbody>
</table>

---

0730  | **Check-in / Poster Setup / Continental Breakfast**                                      |
0830  | Welcome: Mr. David Martinez / MIT Lincoln Laboratory                                     |
0835  | **Mission Keynote Speaker: Convergence of C2 and Combat System – Leveraging SOA**       |
|       | Dr. Michael McGrath / DASN (RDT & E)                                                     |
0905  | **Technology Keynote Speaker: The Impact of Multicore on Math Software**                |
|       | Prof. Jack Dongarra / University of Tennessee, ICL                                       |
0935  | Opening Remarks: Mr. Robert Bond / MIT Lincoln Laboratory                                |
0940  | **Session 1: Multicore Technologies**                                                    |
|       | Chair: Michael Vai / MIT Lincoln Laboratory                                             |
|       | **Auditorium**                                                                           |
0945  | StreamIt—A Programming Language for the Era of Multicores                                |
|       | Saman Amarasinghe / Massachusetts Institute of Technology CSAIL                           |

---

1015  | Break (View Posters)                                                                     |
1030  | **World’s First Polymorphic Computer—MONARCH**                                            |
|       | Lloyd Lewins, Kenneth Prager, Gillian Groves and Michael Vahey / Raytheon Company        |
1100  | **Advanced Programming and Execution Models for Future Multi-Core Systems**             |
|       | Hans Zima / Jet Propulsion Laboratory, California Institute of Technology; Institute of Scientific Computing, University of Vienna, Austria |
**AGENDA**

18 September *(Continued)*

<table>
<thead>
<tr>
<th>Time</th>
<th>Event</th>
</tr>
</thead>
<tbody>
<tr>
<td>1130</td>
<td><strong>Poster / Demo A: Advanced Algorithms and Hardware</strong></td>
</tr>
<tr>
<td></td>
<td><strong>Chair: Michael Vai / MIT Lincoln Laboratory</strong></td>
</tr>
<tr>
<td>1140</td>
<td><strong>Poster / Demo A Précis</strong></td>
</tr>
</tbody>
</table>

**Poster A.1**  
**ALPS: Software Framework for Scheduling Parallel Computations with Application to Parallel Space-Time Adaptive Processing**  
Kyusoon Lee and Adam Bojanczyk / Cornell University

**Poster A.2**  
**A Clustered Multiprocessor and Its Multicore Building Block**  
Matthew Reilly / SiCortex, Inc.

**Poster A.3**  
**NMP ST8 Dependable Multiprocessor**  
John Samson, Jr. / Honeywell, Inc.  
Alan George / University of Florida  
Rafi Some / Jet Propulsion Laboratory, California Institute of Technology

**Poster A.4**  
**DMAGIC: A High-level Partitioning Methodology for Discrete Signal Transforms onto Distributed Hardware Architectures**  
Rafael Arce-Nazario, Manuel Jiménez and Domingo Rodríguez / University of Puerto Rico, Mayagüez

**Poster A.5**  
**TeraByte TokuSampleSort**  
Bradley Kuszmaul / Massachusetts Institute of Technology CSAIL, Tokutek Inc., Cilk Arts Inc., and MIT Lincoln Laboratory

**Poster A.6**  
**Use of Dense Wavelength Division Multiplexing (DWDM) Optical Interconnects to Improve Parallel and Distributed Processing Architecture Connectivity**  
Rick Stevens, Greg Whaley, Roger Karnopp, Howard Schantz and Mert Home / Lockheed Martin Corporation

**Poster A.7**  
**Performance of Direct Attached Disk Subsystems**  
Roger Chamberlain / Washington University in St. Louis and Exegy, Inc.  
Berkley Shands / Washington University in St. Louis

**Poster A.8**  
**When Storage Devices Become Computers**  
Robert Thibadeau and *Kevin Gomez / Seagate Research  
Tom Mitchell and David Touretzky / Carnegie Mellon University  
Terrence Sejnowski / Salk Institute

**Poster A.9**  
**Low Latency Real-Time Computing on Multiprocessor Systems Running Standard Linux**  
Dimitri Sivanich / SGI

**Poster A.10**  
**Optimization of Memory Allocation in VSiPL**  
Jinwoo Suh, Janice McMahon, Stephen Crago and Dong-In Kang / University of Southern California, ISI

**Poster A.11**  
**Use of Python as a Matlab Replacement for Algorithm Development and Execution in a Multi-Core Environment**  
Glen Mabey / Southwest Research Institute  
Brian Granger / Tech-X Corporation

**Poster A.12**  
**Automatic Deployment of Streaming Applications on Hybrid Architectures**  
Roger Chamberlain and Mark Franklin / Washington University in St. Louis

**Poster A.13**  
**Multiprocessor Implementation of a Face Detection System**  
Sankalita Saha / University of Maryland, College Park  
Neal Bamnhva / US Army Research Laboratory  
*Shuvra Bhattacharyya / University of Maryland, College Park

**Poster A.14**  
**Synthesizing Parallel Programming Models for Asymmetric Multi-core Systems**  
Dimitrios Nikolopoulos and Kirk Cameron / Virginia Tech

**Poster A.15**  
**Benchmarking Publish/Subscribe Middleware for Radar Applications**  
Andrew Rhoades, Glenn Schrader and Paul Poulin / MIT Lincoln Laboratory

1225  
**Lunch (View Posters)**

* Denotes presenter other than first listed author
## AGENDA

### 18 September (Continued)

<table>
<thead>
<tr>
<th>Time</th>
<th>Session Title</th>
<th>Speaker(s)</th>
<th>Location</th>
</tr>
</thead>
<tbody>
<tr>
<td>1345</td>
<td><strong>Session 2: Runtime Optimization</strong></td>
<td>Chair: Joel Goodman / MIT Lincoln Laboratory</td>
<td>Auditorium</td>
</tr>
<tr>
<td></td>
<td><strong>TX-2500—An Interactive, On-Demand Rapid-Prototyping HPC System</strong></td>
<td>Albert Reuther, Bill Arcand, Tim Currie, Andy Funk, Jeremy Kepner, Matthew Hubbell, Andrew McCabe and Peter Michaleas / MIT Lincoln Laboratory</td>
<td></td>
</tr>
<tr>
<td>1355</td>
<td><strong>Thimble: Design-time Analysis of Multi-threaded System Behavior</strong></td>
<td>Daniel Waddington / Lockheed Martin Corporation</td>
<td></td>
</tr>
<tr>
<td>1425</td>
<td><strong>Preliminary Study toward Intelligent Run-time Resource Management Techniques for Large Multi-Core Architectures</strong></td>
<td>Dong-In Kang, Jinwoo Suh, Janice McMahon and Stephen Crago / University of Southern California, ISI</td>
<td></td>
</tr>
<tr>
<td>1455</td>
<td><strong>Break</strong></td>
<td></td>
<td>View Posters</td>
</tr>
<tr>
<td>1525</td>
<td><strong>HPC Processor Trends from High-end to Volume, Small, Large, Open, or Embedded</strong></td>
<td>David Scott / Intel Corporation</td>
<td></td>
</tr>
<tr>
<td>1550</td>
<td><strong>Research Challenges for the Next Decade</strong></td>
<td>Zachary Lemnios / MIT Lincoln Laboratory</td>
<td></td>
</tr>
<tr>
<td>1620</td>
<td><strong>Closing Remarks</strong></td>
<td>Jeremy Kepner / MIT Lincoln Laboratory</td>
<td></td>
</tr>
<tr>
<td>1650</td>
<td><strong>Adjourn</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1700</td>
<td><strong>Reception</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1800</td>
<td><strong>Banquet Speaker: American Innovator</strong></td>
<td>Mr. Doug Malewicki / AeroVisions, Inc.</td>
<td></td>
</tr>
<tr>
<td>1845</td>
<td><strong>Banquet</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1930</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
19 September

Day 2 at a Glance

0730  Check-in / Poster Setup / Continental Breakfast
0830  Announcements: Mr. Robert Bond / MIT Lincoln Laboratory

Auditorium

0835  Session 3: Multicore Hardware Challenges
0845  Invited Speaker: Anant Agarwal / Massachusetts Institute of Technology CSAIL
0915  Invited Speaker: James Held / Intel Corporation
0945  Invited Speaker: Markus Levy / The Multicore Association and The Embedded Microprocessor Benchmark Consortium
1015  Break
1030  Yongfeng Gu / Boston University
1100  Peter Vouras / The Johns Hopkins University

Poster / Demo B: FPGA Technologies and Applications
1130  Lunch (View Posters)
1235  Session 4: Novel Applications
1335  Invited Speaker: Norman Rubin / ATI Research
1415  Mark Duchaineau / Lawrence Livermore National Laboratory
1445  Nadya Travinin Bliss / MIT Lincoln Laboratory
1515  Break (View Posters)
1545  Panel: Dr. James C. Anderson / MIT Lincoln Laboratory
1715  Adjourn

Session 3: Multicore Hardware Challenges
Chair: Robert Bond / MIT Lincoln Laboratory

0845  The Tile Processor: A 64-Core Multicore for Embedded Processing
Anant Agarwal / Massachusetts Institute of Technology CSAIL

0915  Intel™ 80-core Tera-scale Research Processor
James Held / Intel Corporation

0945  Using Industry Standards to Exploit the Advantages and Resolve the Challenges of Multicore Technology
Markus Levy / The Multicore Association and The Embedded Microprocessor Benchmark Consortium

1015  Break
1030  Focus 3: Cell
Chair: Sharon Sacco / MIT Lincoln Laboratory

1040  FFTC: Fastest Fourier Transform for the IBM Cell Broadband Engine
David Bader and *Virat Agarwal / Georgia Institute of Technology

1110  Implementation of SIGINT Application on CELL-BE
Richard Besler / Black River Systems Company

1140  Performance of a Multicore Matrix Multiplication Library
Frank Lauginiger, Robert Cooper, Jonathan Greene, Michael Pepe and Myra Jean Prelle / Mercury Computer Systems, Inc.

* Denotes presenter other than first listed author
High Performance Embedded Computing Workshop
18 – 20 September 2007

AGENDA

19 September (Continued)

1130  Poster / Demo B: FPGA Technologies and Applications
Chair: Robert Bond / MIT Lincoln Laboratory

1140  Poster / Demo B Précis

Poster B.1  Evaluating Partial Reconfiguration for Embedded FPGA Applications
Ross Hymel, Alan George, *Chris Conger and Herman Lam / University of Florida

Poster B.2  A Streaming FFT on 3GSPS ADC Data using Core Libraries and DIME-C
Robin Bruce / Institute of System Level Integration, Alba Centre
*Malachy Devlin / Nallatech

Poster B.3  Accelerating Algorithm Implementation in FPGA/ASIC Using Python
Tom Dillon, Jeremy Paatela, Guenter Dannoritzer and Scott Hussong / Dillon Engineering, Inc.

Poster B.4  Phase Unwrapping on Reconfigurable Hardware
Sherman Braganza and Miriam Leeser / Northeastern University

Xinming Huang / Worcester Polytechnic Institute

Poster B.6  Accelerating Genome Sequencing 100X with FPGAs
Olaf Storaasli / Oak Ridge National Laboratory

Poster B.7  Prototyping Advanced Military Sensor Systems Using FPGA-to-ASIC Design Flow
J. Ryan Kenny and Jeff Wills / Altera Corporation
Rick Pancoast and Ellis Taliaferro / Lockheed Martin Corporation

Poster B.8  Digital Beam Former Coefficient Management Using Advanced Embedded Processor Technology
J. Ryan Kenny and Argy Krikelis / Altera Corporation

Poster B.9  FPGA Coprocessing in Multi-Core Architectures for DSP
J. Ryan Kenny and Bryce Mackin / Altera Corporation

Poster B.10  Transformation of Sequential Software into Parallel FPGA Hardware: A Case Study Using the SPEC CPU 2006 Benchmarks
Raymond Hoare / Concurrent EDA, LLC

Poster B.11  FPGA-Based Acceleration of an Image Registration Algorithm
Jay Brockman, Daniel Rinzler and Peter Bui / University of Notre Dame
Frank Iannarilli / Aerodyne Research, Inc.

Poster B.12  Applying Open Standards to FPGA IP Interfaces
Shepard Siegel / Mercury Computer Systems, Inc.

Poster B.13  FPGA Based Systolic Array Implementation of QR Transformation Using Givens Rotations
Xiaojun Wang and Miriam Leeser / Northeastern University

1235  Lunch (View Posters)

* Denotes presenter other than first listed author
19 September (Continued)

1335  **Session 4: Novel Applications**
  Chair: David Cousins / BBN Technologies
  Auditorium

  1345  **Projective Transform on Cell: A Case Study**
  Sharon Sacco, Hahn Kim, Sanjeev Mohindra, Peter Boettcher, Chris Bowen, Nadya Travinin Bliss, Glenn Schrader and Jeremy Kepner / MIT Lincoln Laboratory

  1415  **Toward Fast Computation of Dense Image Correspondence on the GPU**
  Mark Duchaineau, Jonathan Cohen and Sheila Vaidya / Lawrence Livermore National Laboratory

  1445  **Analysis and Mapping of Sparse Matrix Computations**
  Nadya Travinin Bliss and Sanjeev Mohindra / MIT Lincoln Laboratory
  Varun Aggarwal / Massachusetts Institute of Technology
  Una-May O’Reilly / Massachusetts Institute of Technology
  CSAIL

  1515  **Break**
  (View Posters)

  1545  **Panel: Multicore Meltdown?**
  Moderator: Dr. James C. Anderson / MIT Lincoln Laboratory

  **Distinguished Panelists:**
  Dr. James Held / Intel Corporation
  Mr. Markus Levy / The Multicore Association and The Embedded Microprocessor Benchmark Consortium
  Mr. Greg Rocco / Mercury Computer Systems, Inc.
  Mr. Kalpesh Sheth / Advanced Processing Group, DRS Technologies
  Dr. Thomas VanCourt / Altera Corporation

1335  **Focus 4: GPUs**
  Chair: Craig Lund / Mercury Computer Systems
  Room S2-180

  1345  **Are Graphics Processors the New Supercomputers?**
  Norman Rubin / ATI Research

  1415  **Benchmarking the NVIDIA 88006TX with the CUDA Development Platform**
  Michael McGraw-Herdeg / Massachusetts Institute of Technology
  *Douglas Enright and B. Scott Michel / The Aerospace Corporation

  1445  **FFTs of Arbitrary Dimensions on GPUs**
  Xiaobai Sun and Nikos Pitsianis / Duke University

  1515  **DARPA Strap-Boy: Fast Hybrid QR-Cholesky Factorization and Tuning Techniques for STAP Algorithm Implementation on Graphics Processor Architectures for Embedded Systems**
  Dennis Healy / DARPA
  *Dennis Braunreiter, Jackie Sillaci, David Boe and Jeremy Furtek / SAIC
  Xiaobai Sun / Duke University

  Transition to the Auditorium

* Denotes presenter other than first listed author
Day 3 at a Glance

0730 Check-in / Poster Setup / Continental Breakfast
0830 Announcements: Mr. Robert Bond / MIT Lincoln Laboratory

Session 5: Multicore Environments
Chair: Robert Bond / MIT Lincoln Laboratory
Auditorium

0835 High Performance Simulations of Electrochemical Models on the Cell Broadband Engine
James Geraci and Sudarshan Raghunathan / Massachusetts Institute of Technology

0915 Sourcery VSIPL++ for the Cell/B.E.
Jules Bergmann, Mark Mitchell, Don McCoy, Stephan Seefeld and Assem Salama / CodeSourcery
Fred Christensen / IBM
Rick Pancoast and Thomas Steck / Lockheed Martin Corporation

0945 Programming Examples that Expose Efficiency Issues for the Cell Broadband Engine Architecture
William Lundgren / Gedae, Inc.
Rick Pancoast / Lockheed Martin Corporation
David Erb / IBM
Kerry Barnes and James Steed / Gedae, Inc.

1015 Break
<table>
<thead>
<tr>
<th>Time</th>
<th>Session</th>
<th>Presenter(s)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1030</td>
<td>PVTOL: A High-Level Signal Processing Library for Multicore Processors</td>
<td>Hahn Kim, Nadya Travinin Bliss, Ryan Haney, Jeremy Kepner, Sanjeev Mohindra, Sharon Sacco, Glenn Schrader and Edward Rutledge / MIT Lincoln Laboratory</td>
</tr>
<tr>
<td>1100</td>
<td>Defense Applications Implemented Utilizing the Parallel Processing Features of Sourcery VSIPL++</td>
<td>Thomas Steck, Rick Pancoast and Ellis Taliaferro / Lockheed Martin Corporation Jules Bergmann / CodeSourcery</td>
</tr>
<tr>
<td>1040</td>
<td>Application-Level Benchmarking with Synthetic Aperture Radar</td>
<td>Chris Conger, Adam Jacobs and Alan George / University of Florida</td>
</tr>
<tr>
<td>1110</td>
<td>A Survey of Multi-Core Coarse-Grained Reconfigurable Arrays for Embedded Applications</td>
<td>Justin Tripp, Jan Frigo and Paul Graham / Los Alamos National Laboratory</td>
</tr>
</tbody>
</table>
20 September (Continued)

1130  Poster / Demo C: Cell / GPU Technologies
      Chair: Robert Bond / MIT Lincoln Laboratory

1140  Poster / Demo C Précis

Poster C.1  Hardware and Compute Abstraction Layers for Accelerated Computing Using Graphics Hardware and Conventional CPUs
            Justin Hensley / Advanced Micro Devices, Inc.

Poster C.2  Gedae Portability: From Simulation to DSPs to the Cell Broadband Engine
            James Steed, William Lundgren and Kerry Barnes / Gedae, Inc.

Poster C.3  Accelerating MATLAB with CUDA
            Massimiliano Fatica / NVIDIA Corporation
            Won-Ki Jeong / University of Utah

Poster C.4  Implementation of Parallel Processing Techniques on Graphical Processing Units
            Brad Baker, Wayne Haney and Charles Choi / General Dynamics

Poster C.5  R-Verify™: Deep Checking of Embedded Code
            James Ezick, Donald Nguyen and Richard Lethin / Reservoir Labs, Inc.
            Rick Pancoast / Lockheed Martin Corporation

Poster C.6  Dependable Multiprocessing with the Cell Broadband Engine
            David Bueno, Matt Clark and John Samson, Jr. / Honeywell, Inc.
            Adam Jacobs / University of Florida

Poster C.7  Chirp Radar Parameter Estimators over Distributed Hardware Structures
            Cesar Aceros-Moreno, Ana Ramirez and Domingo Rodríguez / University of Puerto Rico, Mayagüez

            Catherine Dezan / Université de Bretagne Occidentale
            *Teng Wang / University of Massachusetts

Poster C.9  The Development and Performance Analysis of a Distributed Corner Turn using the AXIS Graphical Software System
            Thomas Litrenta / Radstone Embedded Systems

Poster C.10 Multi-core Programming Frameworks for Embedded Multimedia Applications
             Kaushal Sanghais and Rick Gentile / Analog Devices, Inc.

Poster C.11 Real-time Multi-core PDE-Solvers in LabVIEW
              Shawn McCaslin, Michael Cerna, Michael Chen, Nanxiong Zhang, Bin Wang and Lothar Wenzel / National Instruments

Poster C.12 Announcing PWRficient Processors from PA Semi, the Most Power-Efficient, High-Performance Processors Available
              Pete Bannon / P.A. Semi

Poster C.13 ★ Efficient Memorization Strategies for Object Recognition with a Multi-Core Architecture
             George Viamontes, Mohammed Amduka, Jon Russo, Matthew Craven and Thanh Vu Nguyen / Lockheed Martin Corporation

1235  Lunch (View Posters)

★ Denotes outstanding submission
* Denotes presenter other than first listed author
### 20 September (Continued)

<table>
<thead>
<tr>
<th>Time</th>
<th>Session</th>
<th>Presenters</th>
</tr>
</thead>
<tbody>
<tr>
<td>1345</td>
<td><strong>Session 6: Awards Session</strong></td>
<td>Chair: Jeremy Kepner / MIT Lincoln Laboratory</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Auditorium</td>
</tr>
<tr>
<td>1355</td>
<td><strong>Vforce: Aiding the Productivity and Portability in Reconfigurable Supercomputer Applications via Runtime Hardware Binding</strong></td>
<td>Nicholas Moore and Miriam Leeser / Northeastern University</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Laurie Smith King / College of the Holy Cross</td>
</tr>
<tr>
<td>1425</td>
<td><strong>On-Chip Photonic Communication for High-Performance Multi-Core Processors</strong></td>
<td>Keren Bergman and Luca Carloni / Columbia University</td>
</tr>
<tr>
<td>1455</td>
<td>Break (View Posters)</td>
<td></td>
</tr>
<tr>
<td>1520</td>
<td><strong>Implementation of Polar Format SAR Image Formation on the IBM Cell Broadband Engine</strong></td>
<td>Jeffrey Rudin / Mercury Computer Systems, Inc.</td>
</tr>
<tr>
<td>1550</td>
<td><strong>POD: A Parallel-On-Die Architecture</strong></td>
<td>Dong Hyuk Woo / Georgia Institute of Technology</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Joshua Fryman / Intel Corporation</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Allan Knies / Georgia Institute of Technology</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Marsha Eng / Intel Corporation</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Hsien-Hsin Lee / Georgia Institute of Technology</td>
</tr>
<tr>
<td>1620</td>
<td><strong>Multithreaded Programming in Cilk</strong></td>
<td>Matteo Frigo / Cilk Arts</td>
</tr>
<tr>
<td>1650</td>
<td><strong>Awards</strong></td>
<td>Jeremy Kepner / MIT Lincoln Laboratory</td>
</tr>
<tr>
<td>1730</td>
<td>Adjourn</td>
<td></td>
</tr>
</tbody>
</table>

★ Denotes outstanding submission