Session 1: Novel Hardware Architectures

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# High Performance Embedded Computing: A Historical Perspective

## Computing Systems

<table>
<thead>
<tr>
<th>Year</th>
<th>System</th>
<th>Processor</th>
<th>Nodes</th>
<th>MFLOPS/Watt</th>
</tr>
</thead>
<tbody>
<tr>
<td>1997</td>
<td>Intel Paragon</td>
<td>50 MHz i860</td>
<td>256</td>
<td>0.07</td>
</tr>
<tr>
<td>1998</td>
<td>STAP Processor</td>
<td>40 MHz ADSP 21060</td>
<td>~1000</td>
<td>~1</td>
</tr>
<tr>
<td>1999</td>
<td>AFRL High Performance Computing System</td>
<td>333 MHz PowerPC 603e</td>
<td>384</td>
<td>39</td>
</tr>
<tr>
<td>2000</td>
<td>Improved Space Processor Architecture</td>
<td>266 MHz PowerPC 603e</td>
<td>20 nodes / 40 PowerPCs</td>
<td>30</td>
</tr>
<tr>
<td>2001</td>
<td>Mk48 Torpedo CBASS BSAR</td>
<td>80 MHz ADSP 21160</td>
<td>12 nodes</td>
<td>91</td>
</tr>
<tr>
<td>2002</td>
<td>Distributed Computing</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

## Enabling Technologies

- **Vector Signal and Image Processing Library 1.0 API**
- **MPI-RT standard**
- **Adaptive Computing Systems & Reconfigurable Computing**
- **Data Reorganization forum**
- **VLSI Photonics**
- **High-Performance CORBA**
- **Polymorphous Computing Architectures**
- **Fault tolerant/fault recovery**
- **High-Performance Embedded Interconnects**
  - InfiniBand
  - Serial RapidIO
- **Parallel MATLAB**
- **Cognitive Processing**
- **Integrated ASICs, FPGAs, PIM, and/or prog. devices**
- **Real-Time Linux**
- **VXS: VMEbus Switched Serial**
Session 1: Papers Highlights

Cognitive Information Processing Technology (Invited)
Zach Lemnios / DARPA / IPTO

Cognitive Systems Goals
• Reason
• Learn
• Explain
• Be Aware
• Respond

MIND: Scalable Embedded Computing Through Advanced Processor in Memory (PIM) Architecture (Invited)
Tom Sterling / CalTech / JPL

Processor in Memory
• 10x - 1000x memory BW
• 4x – 10x reduced latency
• >10x power efficiency
• PIM for unmanned space vehicles

MONARCH: A High Performance Embedded Processor Architecture with Two Native Computing Nodes
John Granacki / USC / ISI

DARPA DIS Embedded Computing Benchmarks for Critical Defense Signal Processing Applications
Stephen Shank / Lockheed Martin

Data Intensive System Benchmarks
• Novel DIS architectures
• Applications: pulse comp., sidelobe canceller, digital target generation, and beam steering

Integrated Heterogeneous Processors
• System on a chip architecture
• Flexible VLSI device for stream front-end and threaded back-end processing

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