High Performance Flexible DSP Infrastructure Based on MPI

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Abstract:
Lockheed Martin has developed a platform independent, scalable and reconfigurable Digital Processor (DP) infrastructure for use in multiprocessor environments. This infrastructure is in use within the Small System Processor (SSP) program. This infrastructure provides communication, data flow, processor/algorithm scaling and configuration flexibility. All aspects of communication and processing are reconfigurable without the need to recompile. Pipeline, round robin, or hybrid processing architectures are supported, as well as modifying the number of processors without the need to recompile. This flexibility is provided by the use of text “flow graph” files, which describe a static processor mapping. Multiple flow graphs are supported.

A non-blocking multicast API is also provided. This is used to distribute the DP Stimulus messages to only the processors that are required to participate in processing.

The communication infrastructure provides an efficient mechanism, which decouples algorithm development from the specific details of the data distribution. Algorithm data flow routines support redistributing data from M to N processors with or without data overlap or minimum block sizes. Also provided are M to N corner turn and algorithm corner turn routines. Blocking and Non Blocking API’s are provided.

This infrastructure is highly portable. The infrastructure was developed on CSPI 2841 multiprocessors using MPI as the underlying communication API and VSIPL as the Vector math library. Because it is based on industry standard API’s, this infrastructure can be run on any platform that supports these API’s. This has been validated on Server Class as well as Embedded platforms. No change to code was made, just a recompile for the particular platform.