Delivered Performance Predictions and Trends for RISC processors in Radar Applications

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The Ultimate Performance Machine
Goals of Presentation

- Provide an evaluation of the achieved performance levels of RISC processing nodes in radar applications
  - RT_STAP Benchmark is used as the representative benchmark
  - Evaluation over a 4-5 year span of node technologies

- We’ll then make projections of performance per watt for emerging PPC/AltiVec-based node architectures
  - Evaluation for the generation of technology that will be emerging within the next 1-2 years (2003-2005)
  - Examine where the major bottlenecks are and how much additional delivered performance we may obtain as we address these bottlenecks in a hypothetical node design (2005+)
Throughput has increased by a factor of 5.6-6.4X
- Power per node (PPC + Network Interface) has increased by ~10% over these generations
- Throughput/watt has increased by factor of 5-5.7X
- Overlapping communications and processing would get closer to the upper end of these performance ranges

Reference Data: PPC processor circa 1998-1999


Approximate Moore's Law Gap

0.0 1.0 2.0 3.0 4.0 5.0 6.0 7.0 8.0 9.0 10.0

Throughput Improvement factor
• Throughput per node has made substantial improvements at the application level in the past few generations due to major architectural improvements: AltiVec
  ➢ > 5-6.5X throughput improvement with power per node holding constant
  ➢ Based upon this one application which maps fairly well to the AltiVec processor

• In order to get these benefits, heavy investments in IP (Intellectual Property) must be made
  ➢ Must investigate bottlenecks in the application and develop new routines that break these bottlenecks and exploit a new chip’s architecture (such as AltiVec)
  ➢ In this case the vendor has made those investments in their middleware
  ➢ By and large the application code base required trivial changes to use these new routines...no major structural changes in the code, ie., most of the burden is on the vendor’s middleware

• Although good, these results indicate that we’re not tracking Moore’s Law
  ➢ In 4-5 years only seeing a 5-6.5X improvement not the doubling every 1.5 years as Moore predicted
  ➢ This required a major architectural improvement: AltiVec
  ➢ *Moore doesn’t predict performance per watt*
Performance to date with AltiVec-type RISC + SIMD processors have measured up to the performance expectations

- But, as expected, this has involved a significant IP investment in software
- This investment has been paid for by the vendor and the application has been largely insulated
- RT_STAP benchmark has shown a 5-6.5X improvement in delivered performance per watt using currently available technology

Throughput/node is increasing with every generation

- To date AltiVec has yielded more than a quadrupling at the application level for a given power rating
- Next-generation nodes should track clock increases assuming I/O rates increase at same rate
- Generation after that could provide big step improvement due to architectural improvements in sustained IO per node

Power per node is increasing

- Throughput is absolutely increasing but so is the power
- An improvement in the sustained IO per node should improve the delivered performance
- Challenge for computer system designers is packaging these nodes in dense systems
- Challenge for Radar system designers is cooling these systems on their platforms

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