An Update on CORBA Performance for HPEC Algorithms

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Elements of Performance

- **Simplified (but accurate) execution model:**
  - Latency
    - End-to-end time to transfer one byte
  - Per Byte
    - Extra end-to-end time to transfer each additional byte
  - Total time
    - Latency + Per Byte * Bytes

- **Copies add to Per Byte time**
  - HPEC hardware transfer rates are competitive with local memcpy times (approx. one byte per clock cycle)
  - Result is that any copies kill throughput (but you knew that)
First Benchmarks: Zero Copy Affect on Windows

- **CPUs**
  - 2 GHz Pentium 4M laptop
  - 1 GHz Athlon desktop
  - (2 GHz P4M is 20% faster than 1 GHz Athlon)

- **Transports**
  - Shared memory on Windows
  - 100 Mb Ethernet
Memory Copy Performance

- **Number of Algorithms**
- **Performance varies depending on:**
  - Cache size
  - Cache line size
  - Bytes moved per operation
- **ORB uses most efficient copy algorithm we can discover**
Memory Copy Performance Comparison

- Time Per Byte (ns) vs. Buffer Size (Bytes)
- Graph shows comparison of memory copy performance across different buffer sizes.
Reducing marshaling copies
- Decreases latency for large transfers
- Increases latency for small transfers

Latency increase occurs because there are more system calls from the transport

Scatter/Gather system calls would reduce the number of calls, and potentially the number of transport copies.
Impact on Latency of Eliminating the Marshaling Copies for the Shared Memory Transport

```
Time (µs)
```

```
Transfer Size (Bytes)
```

- Red line: Copy
- Blue line: No Copy
SHRMEM Bandwidth

- Reducing marshaling copies
  - Increases bandwidth for large transfers
  - Reduces bandwidth for small transfers

- Bandwidth reduction occurs because there are more system calls from the transport

- Scatter/Gather system calls would reduce the number of calls, and potentially the number of transport copies.
SHRMEM Bandwidth

Impact on Bandwidth of Eliminating the Marshaling Copies for the Shared Memory Transport

Bandwidth (MB/s)

Transfer Size (Bytes)

Copy
No Copy
CPU Utilization (green: total CPU, red: kernel CPU)

non-ZC, over TCP/Ethnt, notice user CPU (green minus red) for larger data xfers

ZC, over TCP/Ethnt, virtually no user CPU used for larger data xfers
Network Utilization

Network Utilization, ORB over TCP over 100 Mb Ethernet

Normal bench_demo
only seq doubles
Net Util = 89%
CPU = 48%
TCP/Ethnt

Zero Copy bench_demo
only seq doubles
Net Util = 95%
CPU = 42%
TCP/Ethnt
First Benchmarks: Zero Copy Affect on HPEC

- **Internal work-in-progress versions of ZC ORB**
  - Several suboptimal characteristics
    - Underlying transport
      - High latency
      - DMA transfers are 80K blocks

- **Mercury RACEway++**
  - VxWorks host
  - CE-to-CE communications
Comparing Copy Configurations

Network Throughput of Various ORB and Transport Copy Configurations
Total Roundtrip Time (WIP Versions of ZC ORB)
Work Left

- Finalize Zero-Copy version of ORBexpress
- Rewrite underlying transport, expectations:
  - Better latency (> 10 usec)
  - More efficient use of DMA
CORBA is progressing towards HPEC efficiency requirements

Existing CORBA applications can take efficient advantage of HPEC hardware