Algorithm and Programming Considerations for Embedded Reconfigurable Computers

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OBJECTIVES

- Experience and evaluate the learning curve required to become proficient at developing software for the SRC-6e reconfigurable computer.
- Benchmark and compare the performance and correctness of the SRC-6e against computers with traditional architectures.
- Establish libraries of open-source functions.
- Develop a hardware interface between the SRC-6e and a U.S. Navy AN/SPS-65V search radar.
- Develop software for real time processing of radar signals on the SRC-6e.
- Study and experiment with programming languages, methodologies, and environments to move reconfigurable computing closer to the environment most applications developers are already familiar with.
• LINUX CLUSTER OF TWO PCs
• EACH PC HAS
  – TWO 1000 MHZ INTEL XEON® PROCESSORS
  – COMMON MEMORY
  – SNAP PORT TO MULTI ADAPTIVE PROCESSOR (MAP)
• EACH MAP HAS
  – TWO USER-PROGRAMMABLE XILINX VIRTEX-II FPGAs (6 M GATES EACH)
  – ONE XILINX VIRTEX-II CONTROL FPGA (NOT USER PROGRAMMABLE)
  – ON-BOARD MEMORY
  – SNAP PORT TO PC
  – TWO 96-BIT WIDE CHAIN PORTS TO OTHER MAP
• PROGRAMS WRITTEN IN C OR FORTRAN
  – USER IDENTIFIES WHICH PART(S) OF PROGRAM ARE CONVERTED TO FPGA CIRCUITRY FOR (HOPEFULLY) INCREASED EXECUTION SPEED
  – FPGA CODE CAN ALSO BE WRITTEN IN VHDL OR VERILOG
  – FPGA CAN ALSO BE PROGRAMMED SCHEMATICALLY OR WITH IP CORES
SRC-6E ARCHITECTURE (HALF)

μP Board

Intel® μP

L2

MIOC

PCI

Common Memory

SNAP

MAP

Controller

315/195 MB/s (peak)

6x 800 MB/s

On-Board Memory (24 MB)

6x 800 MB/s

FPGA

FPGA

Chain Port To/From Other MAP
800 MB/s

Chain Port To/From Other MAP
800 MB/s
MAP SOFTWARE DEVELOPMENT

- Code for FPGAs is isolated in external function
- SRC compiler translates C source code into Verilog
- Verilog is compiled to FPGA circuitry
- Map can also be programmed with Verilog, VHDL, IP cores, or schematically
- FPGA circuitry deeply pipelined with 100 MHz clock (10 NS)
- Large pipeline fill time (large latency)
- Calls are inserted in the main program to
  - Initialize the map
  - Transfer input data from common memory to on-board memory
  - Call the external function
  - Transfer output data from on-board memory to common memory
  - Release the map (optional)
LIMITATIONS OF MAP C COMPILER

- LIMITED SUBSET OF C LANGUAGE
- LIMITED DATA TYPES (32-BIT AND 64-BIT INTEGERS)
- SNAP PORT DATA TRANSFERS ARE ALWAYS 32-BIT WORDS AND MUST BE ALIGNED ON A 4-BYTE BOUNDARY
- DATA ARRAYS MUST BE ALIGNED ON A 4-BYTE BOUNDARY
- SIX ON-BOARD MEMORY MODULES
- ONE ARRAY PER MEMORY MODULE
- ONE READ OPERATION OR ONE WRITE OPERATION PER MEMORY MODULE PER CLOCK
- NO SUPPORT FOR ACCESS TO CHAIN PORTS

- FUTURE VERSIONS OF MAP C COMPILER WILL FIX SOME, BUT NOT ALL, OF LIMITATIONS
EVALUATING THE SRC-6e AND MAP COMPILER

• EASE OF USE (SOMewhat SUBJECTIVE)
  – ALGORITHM/CODE MODIFICATIONS REQUIRED TO MAKE USE OF MAP
  – LIMITATIONS IMPOSED BY COMPILER
  – LIMITATIONS IMPOSED BY HARDWARE

• TYPICAL MEASURES OF COMPILER PERFORMANCE
  – CODE EXECUTION SPEED
  – OBJECT CODE SIZE (TRANSirates TO FPGA CIRCUIT AREA)

• THE CORDIC ALGORITHM
  – USED TO EXTRACT PHASE INFORMATION FROM AN I/Q-ENCODED (IN-PHASE/QUADRATURE) RADAR SIGNAL
  – USES SUCCESSIVE APPROXIMATION TECHNIQUE TO ESTIMATE ARCTANGENT FUNCTION
  – NUMBER OF ITERATIONS DETERMINES ACCURACY
  – EASILY PIPELINED
  – USES SHIFT AND ADD ALGORITHM, NO MULTIPLICATION OR DIVISION
CORDIC TEST CASES

- **C VERSION USING ONLY INTEL CPUs**
- **C VERSION USING SRC C COMPILER FOR MAP**
  - 32-BIT INTEGER VARIABLES
  - 11 ITERATIONS
  - MOST CLOSELY MATCHES IP CORE NUMBER 2
- **THREE VERSIONS OF MAP CODE GENERATED WITH XILINX IP CORE GENERATOR TOOL**
- **COMMON “MAIN” PROGRAM**
  - CALLS CORDIC ROUTINE 256 TIMES
  - EACH CALL CALCULATES 249984 ARCTANGENTS
- **DATA INPUTS TO CORES ARE 8 BITS WIDE**
- **INTERFACE TO CALLING ROUTINE USES 32-BIT INTEGERS**
1000 MHZ INTEL XEON VERSUS 1000 MHZ XEON + MAP

CORDIC EXECUTION TIME

EXECUTION TIME

FPGA SPACE USAGE

20% DECREASE
REDUCING MAP DATA ACCESS TIME

- ORIGINAL MAP CODE STORES I AND Q INPUT DATA IN SINGLE ARRAY
- ARRAYS ALLOCATED TO MODULES IN ON-BOARD MEMORY, BUT ONLY ONE READ OR ONE WRITE OPERATION CAN BE PERFORMED ON EACH CLOCK CYCLE WITH EACH MEMORY MODULE
- USE OF 2 ARRAYS ALLOCATED TO 2 MEMORY MODULES, ONE FOR I AND ONE FOR Q INPUT DATA, REDUCES DATA ACCESS TIME

- I and Q = 499968 ELEMENTS
- I = 249984 ELEMENTS
- Q = 249984 ELEMENTS
TEST RESULTS

USING SEPARATE ARRAYS TO STORE I AND Q IMPROVES CORDIC EXECUTION TIME AT THE COST OF MORE FPGA SPACE USAGE

EXECUTION TIME

<table>
<thead>
<tr>
<th></th>
<th>C Baseline</th>
<th>I and Q - one array</th>
<th>I and Q - two arrays</th>
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</thead>
<tbody>
<tr>
<td><strong>EXECUTION TIME</strong></td>
<td></td>
<td>10</td>
<td>8</td>
</tr>
<tr>
<td><strong>5% DECREASE</strong></td>
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FPGA SPACE USAGE

<table>
<thead>
<tr>
<th></th>
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</tr>
</thead>
<tbody>
<tr>
<td><strong>FPGA SPACE USAGE</strong></td>
<td></td>
<td>25.0%</td>
<td>20.0%</td>
</tr>
<tr>
<td><strong>9% INCREASE</strong></td>
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</table>
REDUCING MEMORY DATA TRANSFER TIME

• ORIGINAL MAP CODED ALLOCATED ONE 8-BIT I VALUE AND ONE 8-BIT Q VALUE PER 4-BYTE INPUT WORD AND 1 BYTE OF PHASE DATA PER 4-BYTE OUTPUT WORD
  – DATA TRANSFERS FROM COMMON MEMORY TO ON-BOARD MEMORY
    TRANSFER 1 UNUSED BYTE FOR EVERY BYTE OF USEFUL INPUT DATA
  – TRANSFERS FROM ON-BOARD MEMORY TO COMMON MEMORY
    TRANSFER 3 BYTES OF UNUSED DATA FOR EVERY BYTE OF RESULT DATA

• CORDIC WITH DATA PACKING
  – PACK INPUT DATA BEFORE CALLING MAP ROUTINE, 2 I VALUES AND 2 Q VALUES PER 4-BYTE INPUT WORD
  – TRANSFER DATA FROM COMMON MEMORY TO ON-BOARD MEMORY
  – CALL MAP ROUTINE
  – UNPACK DATA INSIDE MAP ROUTINE
  – EXECUTE CORDIC ALGORITHM
  – PACK RESULT DATA, 4 PHASE VALUES PER 4-BYTE OUTPUT WORD
  – TRANSFER DATA FROM ON-BOARD MEMORY TO COMMON MEMORY
TEST RESULTS

EXECUTION TIME

FPGA SPACE USAGE

190% INCREASE

DECREASE IN MEMORY COPY TIME Significantly less than total time require to pack and unpack input and output data
<table>
<thead>
<tr>
<th></th>
<th>PRECISION (BITS)</th>
<th>ITERATIONS</th>
<th>INTERNAL LATENCY (CLOCKS)</th>
<th>CORE CIRCUIT AREA (SLICES)</th>
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<tr>
<td></td>
<td>INPUTS OUTPUT</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CORE 1</td>
<td>8 9 16</td>
<td>11</td>
<td>17</td>
<td>475</td>
</tr>
<tr>
<td>CORE 2</td>
<td>8 9 32</td>
<td>11</td>
<td>17</td>
<td>777</td>
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<tr>
<td>CORE 3</td>
<td>8 9 48</td>
<td>30</td>
<td>36</td>
<td>2604</td>
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## TEST CASE RESULTS

<table>
<thead>
<tr>
<th></th>
<th>TOTAL CIRCUIT AREA (SLICES*)</th>
<th>TOTAL LATENCY (CLOCKS)</th>
<th>CORDIC EXECUTION TIME (SECONDS)</th>
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<tbody>
<tr>
<td>CORE 1</td>
<td>3260</td>
<td>68</td>
<td>7.3</td>
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<tr>
<td>CORE 2</td>
<td>3555</td>
<td>68</td>
<td>-</td>
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<tr>
<td>CORE 3</td>
<td>5450</td>
<td>81</td>
<td>7.5</td>
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<tr>
<td>C CODE</td>
<td>6710</td>
<td>112</td>
<td>7.4</td>
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</table>

*33,792 SLICES AVAILABLE
RESULTS ANALYSIS

• C CODE REQUIRED 2 TO 5 TIMES MORE CIRCUIT AREA
  – 6710 SLICES COMPARED TO 3555 FOR MOST SIMILAR IP CORE
  – APPROXIMATELY 2800 SLICES ADDED TO CORDIC CODE FOR SNAP PORT INTERFACE AND CONTROL
  – 3910 SLICES COMPARED TO 755 SLICES FOR MOST SIMILAR IP CORE
• CIRCUIT AREA LIMITS PROGRAM SIZE
• EXTRA FPGA AREA CAN BE USED FOR LOOP UNROLLING AND PARALLELIZATION TO INCREASE EXECUTION SPEED
• TOTAL EXECUTION TIME IS APPROXIMATELY THE SAME AT 7.4 SEC
• LATENCY FOR C CODE IS ABOUT TWICE THAT OF IP CORES
• LATENCY IS INSIGNIFICANT WITH LARGE DATA BLOCKS
  – Time per loop = (Latency – 1 + Number of Calculations) * 10 ns
  – (112 – 1 + 249984) * 10 ns = 2.5 msec/loop
• CORDIC EXECUTION TIME IS SMALL COMPARED TO TOTAL EXECUTION TIME OF 7.4 SEC
  – 256 loops * 2.5 msec = 0.64 seconds
• MEMORY TRANSFER TIME DOMINATES EXECUTION TIME
  – MEMORY TRANSFER REQUIRE 4 SECONDS AT PEAK TRANSFER RATE
COMPARISON OF MAP PROGRAMMING METHODS

• USE OF MAP C COMPILER
  – LITTLE SPECIAL KNOWLEDGE OF MAP HARDWARE REQUIRED
  – FLEXIBILITY -- PROGRAMMER IMPLEMENTS ALGORITHM AS DESIRED
  – LIMITED TO DATA TYPES RECOGNIZED BY COMPILER
  – LOWEST COST METHOD FOR APPLICATIONS WHERE IP CORES DO NOT EXIST
  – AVOIDS PURCHASE OR ROYALTY COST OF IP CORES WHEN THEY DO EXIST

• USE OF IP CORES
  – REDUCED DEVELOPMENT EFFORT
  – PREVIOUSLY VALIDATED (HOPEFULLY)
  – EASILY RECONFIGURED
  – LOWER LATENCY (PROBABLY NOT SIGNIFICANT)
  – MORE COMPACT CIRCUIT REALIZATION
CONCLUSIONS

• SRC-6E COMPILER ALLOWS C PROGRAMMERS TO ACCELERATE PROGRAMS WITHOUT BEING CIRCUIT DESIGNERS
• PORTING CODE TO MAP REQUIRES BASIC KNOWLEDGE OF MAP HARDWARE
• MAP C COMPILER PRODUCES CODE THAT COMPARES WELL TO CUSTOM IP CORES
• DEVELOPMENT ENVIRONMENT HAS CAPABILITY TO INTEGRATE IP CORES OR CUSTOM CIRCUIT DESIGNS
• OVERALL PERFORMANCE CAN BE LIMITED BY MEMORY TRANSFER TIME BETWEEN COMMON MEMORY AND ON-BOARD MEMORY
• USE OF LARGE DATA SETS AMORTIZES MAP PIPELINE LATENCY ACROSS MANY CALCULATIONS
• APPLICATIONS PERFORMING A LARGE NUMBER OF CALCULATIONS ON EACH DATA SET DERIVE THE LARGEST PERFORMANCE BOOST FROM USING THE MAP