Reconfigurable Computing
MONARCH/MCHIP
High Efficiency Embeddable TeraFlops
Polymorphous Computing Architecture

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Raytheon / USC-ISI

September 29, 2004
MOrrphable Networkeed micro-ARCHitecture
MONARCH System on a Chip
RISC, DRAM, Computing Array, Streaming I/O

- Polymorphous Architecture
  - Multiple programming modes
    - Reconfigurable, streaming DF
    - RISC scalar
    - RISC SIMD (Altivec like)
  - 6 RISC processors
  - Reconfigurable Computing
    - 96 adders fixed and float
    - 96 multipliers
    - 124 dual port memories
    - 248 address generators
  - 12 MBytes on chip DRAM
  - 14 DMA engines
  - RapidIO interface
  - 20 DIFL ports (1.3 GB/s ea)
  - Power 8-50 W (nominal)
  - Throughput 64 GFLOPS peak

- Alternative to ASICS or custom hardware
- Demonstrated for RADAR, COM, EO
- Late algorithm freeze – retains programmability
- Energy efficiency: 3-6 GFLOPS/W

DARPA
Raytheon
Space and Airborne Systems

ISI
Information Sciences Institute
Multiple Computing Modes adapt to application needs:
1) RISC Scalar, 2) Wide Word, 3) Reconfigurable Data Flow
MONARCH Performance on Lincoln Lab Benchmark Suite

Throughput for Kernels Coded

<table>
<thead>
<tr>
<th>Kernel</th>
<th>Data Set 1</th>
<th>Data Set 2</th>
<th>Data Set 3</th>
<th>Data Set 4</th>
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</thead>
<tbody>
<tr>
<td>FIR SVD CFAR</td>
<td>58.61E+9</td>
<td>39.07E+9</td>
<td>32.63E+9</td>
<td>000.00E+0</td>
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</tbody>
</table>

MONARCH Performance on Lincoln Lab Benchmark Suite

Throughput (Flop/s)

- Average
- Data Set 1
- Data Set 2
- Data Set 3
- Data Set 4

Near Peak Performance with balanced Add/Multiply 64 GFLOPS

Throughput GFLOPS

- 6.3
- 4.3
- 3.2

Instructions Executed

- 22037003
- 2786419
- 957500

Clocks

- 33465175
- 4420820
- 21982

Instructions Executed

- RISC
- WideWord Processor
- FPCA

Clocks

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Near Peak Performance with balanced Add/Multiply 64 GFLOPS

- 58
- 39
- 33

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MONARCH Performance on Lincoln Lab Benchmark Suite

Throughput GFLOPS/Watt

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