Hardware Benchmark Results for An Ultra-High Performance Architecture for Embedded Defense Signal and Image Processing Applications

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ClearSpeed’s Multi Threaded Array Processor Architecture – MTAP
## Power Comparison Results

*(Table presented at HPEC 2003)*

<table>
<thead>
<tr>
<th>Processor</th>
<th>Clock</th>
<th>Power</th>
<th>FFT/sec /Watt</th>
<th>PC/sec/ Watt</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mercury PowerPC 7410</td>
<td>400 MHz</td>
<td>8.3 Watts</td>
<td>3052</td>
<td>782.2</td>
</tr>
<tr>
<td>WorldScape/ClearSpeed 64 PE Chip</td>
<td>200 MHz</td>
<td>2.0 Watts**</td>
<td>56870</td>
<td>24980</td>
</tr>
<tr>
<td>Speedup</td>
<td>----</td>
<td>----</td>
<td>18.6 X</td>
<td>31.9 X</td>
</tr>
</tbody>
</table>

**2.0 Watts was the worst case result from Mentor Mach PA Tools.**

Actual Measured Hardware Results < 1.85 Watts

HPEC 2003 Cycle Accurate Simulations were validated on actual hardware. Results matched to within 1%.
Benchmark

- **Pulse Compression Input (MatLab)**
  - 1 KHz PRF (1ms PRI)
  - 20 MHz sampling rate
  - 870 samples
  - Echo
    - 10 us pulse
    - LFM chirp up
    - 200 samples

- **Pulse Compression Reference (MatLab)**
  - Frequency Domain Reference
  - 10 us
  - LFM chirp up
  - 1024 samples
  - Hamming weighting
  - Bit-reversed to match optimized implementation

- **Pulse Compression Output (MatLab)**
  - 671 samples out of PC
Benchmark Measurements:
Validate Pulse Compression performance with hardware and with data flowing from and to external DRAM (1 MTAP processor)

1) Input Data and reference Function loaded from Host onto DRAM
2) Data input from DRAM to MTAP #1, processed, and output into DRAM
3) Results returned to Host for display
Benchmark Measurements:

Validate Pulse Compression performance with hardware and with data flowing from and to external DRAM
(Average Performance across 2 MTAP processors)

1) Input Data and reference Function loaded from Host onto DRAM
2) Data input to MTAP #1 and (via MTAP #1) to MTAP #2, processed, and output (via MTAP #1) into DRAM
3) Results returned to Host for display
Summary

Hardware validation of HPEC 2003 results to within 1%

**World-class radar processing benchmark results**

Optimized Pulse Compression functions modified using COTS SDK and integrated onto Host platform

**Wide Ranging Applicability to DoD/Commercial Processing Requirements**

- VSIPL Core Lite Libraries under development

  **Application Areas**

  - Image Processing
  - Signal Processing
  - Compression/De-compression
  - Encryption/De-cryption
  - Network Processing
  - Search Engine
  - Supercomputing Applications