HPEC 2004 Panel Session:
Amending Moore’s Law for Embedded Applications

The Second Path: The Role of Algorithms in Maintaining Progress in DSP

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Digital Signal Processing is …

• “… That discipline which has allowed us to replace a circuit previously composed of a capacitor and a resistor with two anti-aliasing filters, an A-to-D and a D-to-A converter, and a general purpose computer (or array processor) so long as the signal we are interested in does not vary too quickly.”

– Prof. Tom Barnwell, Georgia Tech
Reliance on Moore’s Law

• Doing our signal processing digitally has allowed us to grow our capability with Moore’s Law …

... but puts our rate of growth at risk if it begins to falter
Elements Contributing to Embedded Processor Performance

The software side of DSP provides another path to exponential growth in capability
Moore’s-Law Equivalent Years Required to Match FFT Computational Speedup

![Graph showing the relationship between years of hardware improvement required for equal computational speedup and radix-2 FFT length.](image)

- **Y-axis:** Years of Hardware Improvement Required for Equal Computational Speedup
- **X-axis:** Radix-2 FFT Length

The graph illustrates how the years of hardware improvement required increase with the FFT length.
Different Character of Hardware (IC) vs. Algorithm Improvements

<table>
<thead>
<tr>
<th>Improvement Metrics</th>
<th>Hardware</th>
<th>Algorithms</th>
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<tbody>
<tr>
<td>Regularity</td>
<td>Predictable</td>
<td>Unpredictable</td>
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<tr>
<td>Dependent variable</td>
<td>Time</td>
<td>Order complexity</td>
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<td>Impact on applications</td>
<td>Incremental</td>
<td>Leap-ahead</td>
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<tr>
<td>Useful lifetime</td>
<td>3 years or less</td>
<td>10 years or more</td>
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<tr>
<td>R&amp;D Cost growth</td>
<td>2x in 3 years</td>
<td>1.11x in 3 years</td>
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Types of Algorithm Contributions

• Improved efficiency of existing functionality
  – Quicksort, FFT: $N^2 \rightarrow N \log N$
  – Fast multipole algorithm: $N^2 \rightarrow N$

• Architecture-aware implementations
  – FFTW: discrete Fourier transforms
  – ATLAS: linear algebra
  – SPIRAL: DSP algorithms

• Entirely new Functionality
  – Creates capability not achievable with any amount of hardware speedup
  – Example: voice recognition using parametric modeling and HMMs instead of vocoders and 1960s pattern recognition
  – Wavelets, quantum signal processing, nonlinear techniques, knowledge-based and cognitive techniques, etc.
Wafer-Fab Capitalization Cost Compared to Annual DSP Algorithm R&D Costs

- Capital cost for state-of-the-art wafer fab facility
- Annual R&D support for entire IEEE DSP Society membership (18,500 x $150K in 2001)

1.11x every 3 years†
2x every 3 years

† Salary inflation rate based on US Bureau of Labor and Statistics Median Engineering Salaries 1983-2003
Algorithms Provide …

• The other half of implementation speedup

• Entirely new functionality

• Non-exponential cost growth

• A way forward if hardware speedups slow!