Sustaining Moore’s Law with A Super FPGA - Challenges and Solutions

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Computational Platform to Sustain Moore’s Law In the Long Run

KEY CRITERIA

• Exploit Parallelism - Sharing/Reuse not important

• Exploit Modularity - No global clocks

• Avoid Centralized communication structures like register files, caches and memories and replace by scalable, user-programmable data forwarding networks

• High-level Language based tools
- Parallelism
- Reduced control overhead
- Statically configurable interconnect
- Frequency and voltage differentiation
Super-FPGA Architecture

- Core-sized Tile Running @10X freq.
- Pipelined Interconnect
- Pipelined Interconnect @slower freq.
- Mixed Clock FIFO