Super-pipelined CORDIC Unit
With Application to Power System Analysis

Presenter: Prawat Nagvajara

Authors: Michael Fitzharris, Jeremy Johnson, Servesih Tiwari, Prawat Nagvajara
Drexel University

This work is supported by the United States Department of Energy (DOE) under Grant No. CH11171

Center for Electric Power Engineering
Synopsis

• In applications such as power system analysis (e.g., the load flow computation) FPGA hardware to accelerate sine and cosine functions offers a cost-effective solution
• In these applications the host can stream a set of angles to the hardware which streams back the sine and cosine
• CORDIC (COordinate Rotation DIgital Computer) Pipeline structure allows maximal clock speed
• With host/FPGA interconnection, e.g., PCIX, FPGA implementation can provide an order of magnitude speedup over general-purpose personal computer
## Load Flow Computation

**Power flow equations**

\[
P_i = \sum_{k=1}^{n} |V_i| |V_k| \left( G_{ik} \cos (\theta_i - \theta_k) + B_{ik} \sin (\theta_i - \theta_k) \right) \quad i = 1, 2, 3, \ldots, n
\]

\[
Q_i = \sum_{k=1}^{n} |V_i| |V_k| \left( G_{ik} \sin (\theta_i - \theta_k) - B_{ik} \cos (\theta_i - \theta_k) \right) \quad i = 1, 2, 3, \ldots, n
\]

<table>
<thead>
<tr>
<th>System</th>
<th>Branches</th>
<th>NNZ YBUS</th>
<th>NNZ Jacobian</th>
<th>Jacobian Size</th>
</tr>
</thead>
<tbody>
<tr>
<td>1648 Bus</td>
<td>2,602</td>
<td>6,680</td>
<td>21,196</td>
<td>2,982</td>
</tr>
<tr>
<td>7917 Bus</td>
<td>13,014</td>
<td>32,211</td>
<td>105,522</td>
<td>14,508</td>
</tr>
<tr>
<td>10279 Bus</td>
<td>14,571</td>
<td>37,755</td>
<td>134,621</td>
<td>19,285</td>
</tr>
<tr>
<td>26829 Bus</td>
<td>38,238</td>
<td>99,225</td>
<td>351,200</td>
<td>50,092</td>
</tr>
</tbody>
</table>
CORDIC Example

\[
\begin{bmatrix}
x' \\
y'
\end{bmatrix} = \begin{bmatrix}
\cos(\theta) & \sin(\theta) \\
-\sin(\theta) & \cos(\theta)
\end{bmatrix} \begin{bmatrix}
x \\
y
\end{bmatrix} = \cos(\theta) \begin{bmatrix}
1 & \tan(\theta) \\
-\tan(\theta) & 1
\end{bmatrix} \begin{bmatrix}
x \\
y
\end{bmatrix}
\]

Desired angle 28 deg.

Initialization
\[x = 1\]
\[y = 0\]
\[\alpha = 0 \text{ deg.}\]

First Rotation
\[x_{\text{new}} = x - \frac{y}{1} = 1\]
\[y_{\text{new}} = \frac{x}{1} + y = 1\]
\[\alpha = 45 \text{ deg.}\]

Second Rotation
\[x_{\text{new}} = x + \frac{y}{2} = 1.5\]
\[y_{\text{new}} = -\frac{x}{2} + y = 0.5\]
\[\alpha = 18.44 \text{ deg.}\]

Third Rotation
\[x_{\text{new}} = x - \frac{y}{4} = 1.375\]
\[y_{\text{new}} = \frac{x}{4} + y = 0.875\]
\[\alpha = 32.47 \text{ deg}\]
Super-Pipelined CORDIC

Angle Input

Stage 1 (Initialization)

Stage 2 (Shift)

Stage 3 (Add)

Stage 42 (Shift)

Stage 43 (Add)

Trig. Output
Current Implementation

- DMA transfers occur between the host PC and FPGA in both directions
- Software running on the host PC handles all other calculations
• The benefit of the VPF1 board are the dual external Power PC processors which are well equipped to handle the Jacobian construction.

• The CORDIC Processor will be implemented on either of the two on-board FPGAs.

• A 125 MHz PCI bus will be used for the communication, which can reach its full frequency potential due to the FPGA's priority.
Projected Performance

Architecture Speedup

- Tsunami CORDIC Accelerator
- VPF1 CORDIC Accelerator
- VPF1 Hardware Design (ext. PowerPC)
- VPF1 Hardware Design (int. PowerPC)