Xilinx’s Virtex-II Pro FPGA integrates embedded PowerPC processors and reconfigurable logic on a single chip.

We map a Software Defined Radio application to a Virtex-II Pro FPGA.

Application serves as a vehicle to investigate the following:
- PowerPC Processor Local Bus (PLB) Interface
- PowerPC On-Chip Memory (OCM) Interface
- PowerPC Cache

The types of data that are communicated over these interfaces effect an application’s performance.
FM3TR Application Overview

- Use multiple implementations of the FM3TR Application
- Each implementation uses a unique memory configuration

Memory
- On Chip Memory (OCM)
  - Data/Instruction-Side
  - Processor Local Bus (PLB)
  - Data/Instruction-Side

Data
- Application Data
  - Input/Output
- Program Data
  - Stack/Heap
- Instruction Data
  - PPC Instructions
Results

• Appropriate interface selection can improve the performance of an application
• The OCM and PLB interfaces deliver comparable performance
• The OPB delivers performance that is comparable to the PLB in specific scenarios
• Data that exhibits certain attributes should be communicated over one interface versus another
  – Spatial Locality
  – Temporal Locality
• Use of the PowerPC’s cache can hurt an application’s performance