FPGA Implementation of MIMO Wireless Receiver in An Interference Environment

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MIMO Communication
Multiple-Input Multiple-Output

- MIMO Benefits to Communication Link
  - Transmit spatial diversity
  - Beamforming gain
  - Spatial jammer mitigation
Receiver Architecture and Implementation Issues

Goals
- Jammer mitigation
- Synchronization
- Real-time MIMO receiver

Implementation
- QR decomposition / Back substitution
- Multi-channel correlation
- Multiple decision-feedback beamformers

**Diagram:**
- 4 Channel ADC
- Supplied with Digital Hardware
- Designed and Implemented @ Lincoln Laboratory
- Commercially Available Viterbi Decoder

Issues & Requirements
- Rapid prototyping (6 months)
- Concurrent design fine-tuning and FPGA coding
- SDR hardware resource limitation
- 2 transmitter x 4 receiver
FPGA Implementation and Results

**Receiver Architecture**

- **DIQ**
- **Back sub**
- **QRD**
- **Sync**
- **Beam former**
- **Decoder**

**Beamformer IQ Constellations**

**BF#1**

- Synthetic Data Parameters
  - 4 dB SNR signal
  - 30 dB JSR jammer

**BF#2**

**Digital Board**

- 6.0 inches
- 5.0 inches

**Successful real-time signal processing**

**Usage of Altera EP1S30**

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<tr>
<th></th>
<th>Clock</th>
<th>L.E.</th>
<th>Mult.</th>
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<tbody>
<tr>
<td>QR/Backsub</td>
<td>112 MHz</td>
<td>24%</td>
<td>66%</td>
</tr>
<tr>
<td>Beamformer</td>
<td>112 MHz</td>
<td>77%</td>
<td>91%</td>
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<tr>
<td>Sync.</td>
<td>56 MHz</td>
<td>28%</td>
<td>4%</td>
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