Portable and Scalable Supercomputing

Meeting the Needs of HPEC with PIM

Poster Session B.14: 9/21/05
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CPU Technology, Inc.
Application Specific Multi-Core Solutions

- Founded in 1989
- World Class Customer Base
- A History of Growth and Profitability
- Major Investor: The Carlyle Group

20 processors on a single SOC flying in F-16 aircraft today!
Meeting Today’s Needs

- A Growing need for Cost Effective Autonomous Intensive Compute Capacity Close to the Sensor

- Customers have Critical Requirements
  - Performance, Size, Weight & Power Requirements
  - Security (Anti-Tamper)
  - Reliability & Fault Tolerance

**HPEC User Community**

A Scalable, Deeply Coupled (PIM) Processor In Memory Architecture

- Backward compatible
- Low power, small form factor
- Ultra-low component count
- Integrated Security (protected on-chip execution)
- Trusted, on-shore, end-to-end process
- Concentrated General-Purpose Compute Power

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Multi-Core PIM Can Address the Challenge

• **Security:**
  - On chip storage and execution along with additional security features minimizes external tamper susceptibility

• **Cost Effective & SWAP :**
  - Innovative Host/Task Processor Architecture Minimizes Modification of Target Application
  - Compatible to Existing Systems
  - Ultra Low Part Count Vastly Increases Reliability while Reducing Power Consumption

• **Performance :**
  Unprecedented Memory and Processor-to-Processor Bandwidth