An FPGA API for VSIPL++

Authors:
Ben Cordes, Kris Kieltyka, Miriam Leeser, Joe Tarkoff
(Northeastern University)
M. Michael Vai (MIT Lincoln Labs)

Project goals:
- Allow the VSIPL++ programmer to use reconfigurable hardware without needing to program it manually
- Emphasize high performance with minimal overhead
- Very few code changes required
- “Drop-in” replacement for current VSIPL++ algorithm classes (FFT, FIR, etc.)
Example Code

VSI PL++ (software only)

```cpp
FFT<const_Vector, cscalar_f, cscalar_f, FFT_FWD>
    fft_obj(Domain<1>(16), 1.0);
Out = fft_obj(In);
```

VSI PL++ with FPGA support

```cpp
WildcardII *board1 = new WildcardII;

HW_FFT<const_Vector, cscalar_f, cscalar_f, FFT_FWD, SERIAL>
    fft_obj(Domain<1>(16), 1.0, board1);
Out = fft_obj(In);
```
What’s Under The Hood?

- VSIPL++ Data Types
- VSIPL++ Software Algorithm Object (interchangeable)
- VSIPL++ Hardware Algorithm Object
- FPGA HW Object
- FPGA Board

Interface between Algorithm and Board objects is generic, to ease development of new objects.

- Initialize Board API
- Pick FPGA program from library of bitstreams
- Convert data types

Use Board API to:
- Program/Reset board
- Set clocks
- Send/Receive data
- Run algorithm