An FPGA API for VSIPL++

Authors:

Ben Cordes, Kris Kieltyka, Miriam Leeser, Joe Tarkoff
(Northeastern University)

M. Michael Vai (MIT Lincoln Labs)

Project goals:

- Allow the VSIPL++ programmer to use reconfigurable hardware without needing to program it manually
- Emphasize high performance with minimal overhead
- Very few code changes required
- “Drop-in” replacement for current VSIPL++ algorithm classes (FFT, FIR, etc.)

Example Code

VSIPL++ (software only)

```
FFT<const_Vector, cscalar_f, cscalar_f, FFT_FWD>
   fft_obj(Domain<1>(16), 1.0);

Out = fft_obj(In);
```

VSIPL++ with FPGA support

```
WildcardII *board1 = new WildcardII;

HW_FFT<const_Vector, cscalar_f, cscalar_f, FFT_FWD, SERIAL>
   fft_obj(Domain<1>(16), 1.0, board1);

Out = fft_obj(In);
```

What's Under The Hood?