Benchmark Results for Ultra-High Performance Scalable Processing Architecture for Embedded Signal and Image Processing Applications

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1024-point complex Pulse Compression

- **Per chip measurements:**
  - 96 PE’s enable 12 sets in parallel
    - 8 PE’s per PC
  - 9.39 usec DRAM to DRAM
  - 9.87 usec on-chip (ie without I/O from/to DRAM)
  - 11.55 GFLOPS with I/O
  - 11.02 GFLOPS without I/O

- Overlapping of I/O and compute results in **95%** of cycles being used for computation
## Pulse Compression Demonstration
### Hardware Performance

<table>
<thead>
<tr>
<th>Routine</th>
<th>Buffer (12 signals)</th>
<th>1K signal</th>
<th>Time</th>
<th>Rate (signals/sec)</th>
</tr>
</thead>
<tbody>
<tr>
<td>FFT</td>
<td>12.7K cycles</td>
<td>1.06K cycles</td>
<td>4.23 usec</td>
<td>236K (fft only)</td>
</tr>
<tr>
<td>CM</td>
<td>2.2K cycles</td>
<td>0.18K cycles</td>
<td>0.73 usec</td>
<td>-</td>
</tr>
<tr>
<td>IFFT</td>
<td>13.3K cycles</td>
<td>1.11K cycles</td>
<td>4.43 usec</td>
<td>226K (ifft only)</td>
</tr>
<tr>
<td>Filter work</td>
<td>28.2K cycles</td>
<td>2.35K cycles</td>
<td>9.4 usec</td>
<td>106K (no I/O)</td>
</tr>
<tr>
<td>DRAM_READ</td>
<td>0.7K cycles</td>
<td>0.06K cycles</td>
<td>0.23 usec</td>
<td>-</td>
</tr>
<tr>
<td>DRAM_WRITE</td>
<td>0.7K cycles</td>
<td>0.06K cycles</td>
<td>0.23 usec</td>
<td>-</td>
</tr>
<tr>
<td>TOTAL</td>
<td>29.6K cycles</td>
<td>2.47K cycles</td>
<td>9.87 usec</td>
<td>101K PC/sec per chip</td>
</tr>
</tbody>
</table>

*Best in World!!*
Scalable Processing Platform™

- ~50 GFLOPS
  64-bit FP
  SIMD Processor Chip

- ~100 GFLOPS
  64-bit FP
  PMC/XMC Daughtercard

- ~300 GFLOPS
  64-bit FP
  6U VME Expansion board

- ~3 TFLOPS
  64-bit FP
  Single Rack SPP
  (30x – Full Duplex 10 GigEthernet)

(x 10)
CamArray™ Multi-Sensor Platform

- 6 Cameras Dual CameraLink (x3)
- 6U Host Motherboard
- 42 Cameras per Cardcage
- With SAN Storage