VSIPL++
HPEC Kernel Benchmarks
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Sourcery VSIPL++ Advantages:

• **Productivity**
  – SIP algorithms can be implemented efficiently and effectively
  – Parallel version of code implemented with few changes to serial version

• **Performance**
  – Utilizes vendor libraries for good performance with low overhead
  – Throughput is nearly the same as the serial version
  – Achieves expected linear speedups for parallel versions

• **Portability**
  – Identical code runs on all supported systems.
  – Reconfigurable to use vendor libraries optimized for a given system

• **Parallelism**
  – Minimal code changes
  – No MPI programming
  – Near-zero performance overhead in serial case
FIR Bank: Serial vs Parallel

Data Set #1 – Fast Convolution
• Run on 64 Xeon processors
• Speedups shown for 4096 points

Data Set #2
• Shows similar speedups

<table>
<thead>
<tr>
<th>CPUs</th>
<th>GFLOP/s</th>
<th>Speedup</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>4.3</td>
<td>1.0</td>
</tr>
<tr>
<td>2</td>
<td>6.3</td>
<td>1.5</td>
</tr>
<tr>
<td>4</td>
<td>10.9</td>
<td>2.5</td>
</tr>
<tr>
<td>8</td>
<td>27.8</td>
<td>6.5</td>
</tr>
<tr>
<td>16</td>
<td>75.1</td>
<td>17.5</td>
</tr>
<tr>
<td>32</td>
<td>161.9</td>
<td>37.7</td>
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<tr>
<td>64</td>
<td>336.8</td>
<td>78.3</td>
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