Implementation of FIR on MONARCH Processor

Jinwoo Suh and Janice O. McMahon
University of Southern California
Information Sciences Institute
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- MONARCH Processor
  - By Raytheon and USC/ISI
  - Both control flow processors and data flow processors
    - 6 RISCs and 12 ALU clusters
  - Provides high performance
    - 64 GOPS peak ALU performance at 333 MHz
Implementation of FIR on MONARCH Processor

- FIR bank implemented
  - Several sets of FIR in time domain
  - Performance results collected for various number of sets, number of input data, and number of coefficients

\[ y_m[i] = \sum_{k=0}^{K-1} x_m[i-k]w_m[k], \text{ for } i = 0,1,\ldots,N-1 \]
Implementation of FIR on MONARCH Processor

• FIR Implementation
  – Manual coding using MONARCH assembly language
  – Obtained high efficiency of 99.9%

• Conclusion
  – Perfect match between MONARCH and FIR computational requirement
  – High performance on FIR obtained
  – Very good scalability
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