Field Programmable Multi-cores: A New Class of Semiconductors

Gail Walters
High Performance Embedded Computing Workshop
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A global market perspective of generational processing technology.

(Includes embedded, general and special purpose applications.)

Market Expansion from:
Increased Function, Capacity and Performance
Decreased System Price

85% of system behavior is contained in software.
Two distinct family groups both fabricated on-shore with the NSA TAPO / IBM Trusted Foundry.
Enabling Software Compatible Transformation

Point and Click to configure

Visibility / System Level Tools

Compatible Integration & Performance

SystemLab™
Acalis™ FPMC
Field Programmable Multi-Core Products

Addressing SW Compatibility

IBM Trusted Foundry
Acalis™ Software Compatibility

Compatible Integration & Performance
Field Programmable System-on-Chip Example (MOAC)

- 20 Processors
- 2.5 Megabits RAM
- 12 DMA controllers
- 12 Timers
- Multiple interfaces
- Dual 1553 controllers
- Ethernet Controller
- Split Transaction Bus
- On Chip – BIST
- AT Security Features
Acalis™ FPMC
Field Programmable Multi-Core Products

Addressing Scalable Performance

IBM Trusted Foundry
QChip is a MultiCore and Memory semiconductor......
Multi-Core in Memory Array
32 QChips  4 x 4 x 2 Mesh Architecture

- 64 x 128bit Memory Ports
- Embedded DRAM 256 - 512MBytes
- 64 PowerPC Compatible Processors
- 64 Floating Point Co-Processors
- 667Mhz
- 64 Communication Processors with Hardware Barrier Synchronization

Performance/Watt – >10X
SystemLab™ Software Debug Interface
IBM Trusted Foundry – 90nm
1024 x 64 bit Streaming Registers per CPU
Multi-Core in Memory Array (Stick)

4 QChips 2 x 2 Mesh Architecture

- 8 x 128bit Memory Ports
- Embedded DRAM 32 - 64MBytes
- 8 PowerPC Compatible Processors
- 8 Floating Point Co-Processors
- 667Mhz
- 8 Communication Processors with Hardware Barrier Synchronization
- Performance/Watt – >10X
- SystemLab™ Software Debug Interface
- IBM Trusted Foundry – 90nm
- 1024 x 64 bit Streaming Registers per CPU

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Operating System Processors

Application Processors
Behavioral System View

Shared Memory Architecture

64 Ports of 72 Bit DDR 333 (64 + ECC) and 64 Ports of 144 Bit eDRAM 667 (128 + ECC)
Minimum 256MB / port – 16.5 GBytes

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SuperQ–64™
General Purpose Industry Leading Compatible Server Blade

SuperQ–64™Server
- Performance: ~100,000 DMIPS
- Processors: 64 PowerPC Cores & Dual Opterons
- Power: 1 KWatt
- DRAM: 32 Gbytes
- Disk: 1 Terabytes
- OS: NSA Linux
- Architecture: Shared Memory 3D Mesh
SuperQ-64™
General Purpose Industry Leading Compatible Server Blade

TOTAL COST OF OWNERSHIP / DMIP

FLOOR SPACE (NUMBER OF 7 FOOT RACKS)

(10 Blade Configuration –Super-Q-64)
CPU TECH Configuration
X86 and PowerPC Compatible
900,000 DMIPS
680 GB DRAM
7.5 TB Disk

(168 Dual Processor Blade Configuration)
All others Configuration
X86 Compatible
676,000 DMIPS
672 GB DRAM
6.5 TB Disk
Industry Leading Design Automation System Tools
System Level Simulation & Visibility

SystemLab™
Acalis™ FPMC
Field Programmable MultiCore Products

- World Class IBM and CPU Tech IP
- Includes Legacy Processors and Multiple PowerPCs
- Trusted Foundry On Shore
- Security Features
- Field Programmable & Field Configurable
- Multiple I/O Engines (From GHz class to 1553)
- SystemLab™ Interface
- Communication Processors
- High Performance DDR Interfaces with ECC
- Designed for Extreme Environments

First Software Compatible in Production
First Scalable Performance System in Development – Prototype in Nov06
Chips in Oct 07
Second Software Compatible in Development
“A lot of things are technologically possible, but only economically feasible products will become a reality.”

- Robert Noyce
Founder, Intel

from time to TIME...

a company comes along that is uniquely positioned to lead the way into the next generation by offering the right solution for the right price at the right time.

CPU TECH
Compatible Systems, Technology & Services