HPEC: Looking Back and Projecting Forward

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2006 High Performance Embedded Computing Workshop

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Outline

• Big Picture Over Past Decade
  • HPEC Representative Developments
  • DoD Landscape and Impact on HPEC
  • The Next Decade and Net-Centric Architectures
  • Summary
World Events and Directives Impacting DoD Investments

- Post-cold war era begins
- Persian Gulf war
- World Trade Center bombing
- U.S. Embassy bombings (Kenya, Tanzania)
- U.S.S. Cole attack
- 9/11 attack
- Afghanistan/Iraq Wars
- U.S. abandons 30 year-old antiballistic missile treaty
- Multiple terrorist attacks worldwide (Bali, Madrid, London, Jordan)


- Doing more with less (decrease in DoD budget)
- Capability-based acquisition
- Transformation

- ‘Last supper’ (shrinking of the industrial base)
- Total System Performance Responsibility (TSPR directive)
- Army establishes Lead System Integrator for FCS

Several large programs began: FIA; FCS; SBIRS-HIGH; ...
DoD Budget and QDR Focus

- **DoD Budget**
  - Actuals & Estimates $B
  - 1990: 200
  - 1995: 300
  - 2000: 400
  - 2005: 500
  - 2010: Unlikely to hold

- **QDR Focus**
  - 2001 Quadrennial Defense Review (from threat-based to capability-based acquisition)
  - 2005 Quadrennial Defense Review

- **DoD Software**
  - Application
  - Middleware
  - Embedded SW Standards

- **COTS development**
  - Vendor SW
  - 1990
  - 2000
  - 2005

- **Security Challenges**
  - Irregular
  - Lower Vulnerability
  - Traditional
  - Lower Likelihood
  - Catastrophic
  - Higher Vulnerability
  - Disruptive
  - More Likely

*Source: U.S. Office of Management and Budget*
## High Performance Embedded Computing
- A Historical Perspective -

<table>
<thead>
<tr>
<th>Year</th>
<th>Computing Systems</th>
<th>Enabling Technologies</th>
</tr>
</thead>
<tbody>
<tr>
<td>1997-1998</td>
<td>Intel Paragon &amp; STAP Processor</td>
<td>• VSIPL &amp; MPI standards</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Adaptive Computing Systems / Reconfigurable Computing</td>
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<tr>
<td></td>
<td>AFRL HPCS &amp; Improved Space Processor Architecture</td>
<td>• Data Reorg forum</td>
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<tr>
<td></td>
<td></td>
<td>• High-performance CORBA</td>
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<tr>
<td></td>
<td></td>
<td>• VLSI Photonics</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Polymorphous Computing Architectures</td>
</tr>
<tr>
<td></td>
<td>NEC Earth Simulator &amp; Mk 48 CBASS BSAR</td>
<td>• High-performance embedded interconnects</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Parallel MATLAB</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Cognitive Processing</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Integrated ASICs, FGPAs, and prog. devices</td>
</tr>
<tr>
<td></td>
<td>LLGrid System &amp; KASSPER</td>
<td>• Grid computing</td>
</tr>
<tr>
<td></td>
<td>IBM Blue Gene &amp; WorldScape Scalable Processing Platform</td>
<td>• VXS (VME Switched Serial) draft standard</td>
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<tr>
<td>2005-2006</td>
<td>Net-centric / service-oriented architectures &amp; unmanned platforms</td>
<td>• VSIPL++ standard</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Multi-core processors</td>
</tr>
<tr>
<td>2007+</td>
<td></td>
<td>• Self-organizing wireless sensor networks</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Global Information Grid</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Distributed computing and storage</td>
</tr>
</tbody>
</table>
## HPEC Workshop Highlights

### 1997
- keynote: RADM K. Paige, USN
- 1st HPEC
- VSIPL API v1.0 released

### 1998
- keynote: F. Perry, SPAWAR
- 1st session dedicated to reconfigurable computing
- MPI/RT API v1.0 released

### 1999
- keynote: D. Tennenhouse, DARPA
- banquet: T. Sterling, JPL
- 1st banquet speaker

### 2000
- keynote: C. Holland, DUSD
- banquet: C. Williams, JPL
- 1st BAA/program announcement

### 2001
- keynote: G. Bell, Microsoft
- banquet: T. Knight, MIT AI Lab
- 1st session dedicated to parallel MATLAB

### 2002
- keynote: Maj Gen P Nielsen, USAF
- banquet: Cleve Moler, The Mathworks
- 1st VSIPL++ talk

### 2003
- keynote: J. Parmentola, ADRLM
- banquet: R. Kurzweil, Kurzweil Technologies
- 1st US-only session

### 2004
- keynote: D. Patterson, UC Berkeley
- banquet: M. Flynn, Stanford
- Grid computing

### 2005
- keynote: Brig Gen G. Connor, USAF
- banquet: M. Cusumano, MIT
- Cell processor

![Graph showing MOPS per W over time with exponential growth](image-url)
Outline

• Big Picture Over Past Decade

→ • HPEC Representative Developments

• DoD Landscape and Impact on HPEC

• The Next Decade and Net-Centric Architectures

• Summary
A Decade of Embedded Computing

Late 1980s - Early 1990s
- Custom design
- COTS parts
- Non-portable SW
- Application specific prototype demonstration

Mid-Late 1990s
- COTS HW
- Vendor specific SW
- Portable SW library
- Legacy SW
- June 1994- Sec. Def. Perry reduces reliance on military specs and standards: go commercial

Early 2000s - Mid 2000s
- Balanced architectures
- Custom front-end HW followed by COTS back-end
- SW standards
- Leverages information technology from commercial sector

MIT Lincoln Laboratory
# Early 90’s Space-Time Adaptive Processor

## Hardware Overall Complexity

<table>
<thead>
<tr>
<th>Component Type</th>
<th>Total Size</th>
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<tbody>
<tr>
<td>IC (LSI and VLSI)</td>
<td>≈ 25,000</td>
</tr>
<tr>
<td>Unique Custom Board Designs</td>
<td>13 Board Designs</td>
</tr>
<tr>
<td></td>
<td>I/O 288 Pins</td>
</tr>
<tr>
<td></td>
<td>≈ 200 ICs</td>
</tr>
<tr>
<td></td>
<td>125 Square Inches</td>
</tr>
<tr>
<td>Total Boards</td>
<td>134 Boards</td>
</tr>
<tr>
<td></td>
<td>113 Printed Circuit</td>
</tr>
<tr>
<td></td>
<td>21 Wire Wrap</td>
</tr>
<tr>
<td>Total Chassis</td>
<td>14</td>
</tr>
<tr>
<td></td>
<td>11 Real-Time Signal Processing</td>
</tr>
<tr>
<td></td>
<td>3 Control</td>
</tr>
<tr>
<td></td>
<td>21 Slot 9U VME</td>
</tr>
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</table>
STAP Processor Top Level Architecture
Custom Design with COTS Components

CUSTOM DESIGN WITH OFF-THE-SHELF COMPONENTS

- HIGH-THROUGHPUT FIR FILTER
  - INMOS A100
  - 400 MOPS
  - 16-BIT DATA INPUT
  - 16-BIT ARITHMETIC
  - 16 COMPLEX TAPS
  - 6.25 MHz CLOCK
  - (8-Bit Coefficients)
  - POWER < 2 W

- COMPLEX MULTIPLIER
  - PLESSEY PDSP16112
  - 16-BIT DATA INPUT
  - 12-BIT COEFFICIENTS
  - 10 MHz CLOCK
  - POWER < 500 mW

- PROGRAMMABLE DSP MICROPROCESSOR
  - TI TMS320C30
  - 33 MFLOPS
  - 32-BIT FLOATING-POINT
  - 60 ns INSTRUCTION
  - 2 K × 32 ON-CHIP RAM
  - 2 SERIAL PORTS
  - 33 MHz CLOCK
  - POWER < 2 W

- DUAL-PORTED RAM
  - INTEGRATED DEVICE TECHNOLOGY
  - IDT 7130
  - 1 K × 8
  - ACCESS TIME 35 ns
  - POWER < 800 mW

- HIGH-PERFORMANCE ALU
  - IDT 7381
  - 16-BIT DATA INPUT
  - 16-BIT ARITHMETIC
  - 10 MHz CLOCK
  - POWER < 300 mW

- CMOS STATIC RAM
  - SHARP LH821002
  - 256 K × 4
  - ACCESS TIME 25 ns
  - POWER < 400 mW
Embedded Real-Time Signal Processor

- Reduction in hardware size
- Flexible waveform design
- High performance digital filtering functions
- 100–1000 billion operations per second

- Massively parallel processor
- Portable signal processing libraries
- Real-time performance
- 50–500 billion floating-point operations per second
Front-End Processor Hardware

Chassis Level Architecture

SBC Force CPU-10
Ethernet
Fibre Channel

DIST. Brd.

CPI PRI BW Signals

DIQ Brd.

Dval Window
Radar Data (4 Channels)

DOB Brd.

To Programmable Signal Processor
To Tape Recording Subsystem

Hardware Features

- Dedicated VLSI
- 100 GOPS
- Two 9U VME chassis
- Form factor:
  - 7.3 ft³
  - 210 lbs
  - 1.5 kW
- Throughput density:
  - 14 GOPS/ft³
VLSI Custom Front-End Chip

ASIC Features
- 2 GOPS
- 585 mil x 585 mil die
- 1.5 Million transistors
- 0.65\textmu\text{CMOS}
- Three-layer metal
- 4 Watts/chip

Performance Results

![Target + Noise Performance](image)
Airborne Signal Processor

**Custom Hardware**
- Dedicated VLSI
- 100 GOPS
- Two chassis
- Form factor
  - 7.3 ft³
  - 210 lbs
  - 1.5 kW
- Throughput density = 14 GOPS/ft³

**AMPEX Tape Recorder**
- Tape recorder rate = 30 Mbytes/sec
- 1 Bit error every 240 CPI
- 25 min cassette capacity
- Recorded data = 30% of available data with 17% waveform

**COTS Programmable Signal Processor**
- SHARC AD21060 based
- 85 GFlops
- Bisection BW = 3.2 Gbytes/sec
- I/O throughput = 240 Mbytes/sec
- Four chassis
- Form factor
  - 33 ft³
  - 812 lbs
  - 6.9 kW
- Throughput density = 2.2 GFLOPS/ft³
Hardware Advances in Signal Processor Systems

1988  89  90  91  92  93  94  95  96  97  98  99  2000  01  02  03  04  05

Adaptive Processor 1992
- 22 GOPS
- 50 ft³
- 1400 lbs
- 8 KW
- 3 MOPS/W

STAP Processor 1998
- 200 GOPS
- 40 ft³
- 1000 lbs
- 8.4 KW
- 22 MOPS/W

AEGIS Surveillance Radar 2000
- 43 GFLOPS
- 110 ft³
- 1960 lbs
- 14 KW
- 3 MFLOPS/W

Missile Seeker 2002
- 16 GFLOPS
- < 1 ft³
- 2 lbs
- 31 W
- 500 MFLOPS/W

Cluster 2005
- 432 GFLOPS
- 46 ft³
- 1200 lbs
- 7.2 KW
- 60 MFLOPS/W

Knowledge Aided Radar 2003
- 16 GFLOPS
- < 1 ft³
- 2 lbs
- 31 W
- 500 MFLOPS/W

200 GOPS 40 ft³ 1000 lbs 8.4 KW 22 MOPS/W

16 GFLOPS < 1 ft³ 2 lbs 31 W 500 MFLOPS/W

432 GFLOPS 46 ft³ 1200 lbs 7.2 KW 60 MFLOPS/W

450 GFLOPS 9 ft³ 325 lbs 1.5 KW 300 MFLOPS/W
Historical Perspective on Systems and Software

20 KOPS to 480 GFLOPS
> Factor 10^7 growth
Outline

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• DoD Landscape and Impact on HPEC
• The Next Decade and Net-Centric Architectures
• Summary
Continuing the reorientation of military capabilities and implementing enterprise-wide reforms to ensure structures and process support the President and the warfighter.
DoD Options and Capabilities Provided

Provide more options for President, capabilities for CoComs

Post-9/11 Security Challenges

- **Irregular**
  - Non-state and state actors employing "unconventional" methods to counter stronger state opponents; terrorism insurgency, etc.

- **Traditional**
  - States employing military forces in well-known forms of military competition and conflict

- **Catastrophic**
  - Terrorist or rogue state employment of WMD or methods producing WMD-like effects against U.S. interests

- **Disruptive**
  - Competitors employing technology or methods that might counter or cancel our current military advantages

Capability Focus Areas

- **Options for President**
  - Defeat terrorist networks
  - Defend homeland in depth
  - Prevent acquisition or use of WMD
  - Shape choices of countries at strategic crossroads (Assure, Dissuade, Deter, Defeat)

- **Capabilities for COCOMs**

Note: From QDR Report, February 6, 2006
Growth in UAV Investment

Note: Adapted from Unmanned Aircraft Systems Roadmap, 2005-2030.
Next Generation Systems Employing Phased-Array Architectures

Challenges Facing Next Generation Systems

- Multi-Function System Capability
  - Programming Flexibility
  - Rapid context switching
- Increase Number of Phase Centers
  - High Computation Throughput
  - High Comm. and Memory
- Very constrained in form factor
  - Small size, weight and power
- Open system architecture
## Functions-Platforms-Sensors Desired

### Functions
- Intelligence
  - Surveillance
    - Space
    - Air
    - Ground
    - Ocean
    - Underwater
    - Subsurface
- Reconnaissance
- Targeting
- Monitoring
- Fire Control
- Guidance
- Communication
- Mapping
- Discrimination
- ATR
- Imaging
- BDA
- Command, Control
- Coordination
- Tasking

### Platforms
- **Land**
  - Fixed sites, Vehicles
  - Personnel, UGS, UGVs
- **AIR**
  - UAVs
    - (large, small, micro)
  - Aircraft, Aerostats,
    - Blimps,
    - Missiles, Shells
- **Sea**
  - Ships,
    - Submarines
    - Underwater Sites,
      - UUV, Torpedoes
- **Space**
  - Rockets
  - Missiles
  - Satellites

### Sensors
- **Coherent Signal**
  - Radar
    - SAR
    - MTI
  - SIGINT
  - Communication
    - RF
    - Laser
  - Seismic
  - Acoustic
- **Non-Coherent Signal**
  - Electro-optic
  - Infrared
  - Multispectral
  - Hyperspectral
  - Ultraspectral
  - Nuclear/
    - Chemical/
    - Biological
Trends in Computing Technology

Memory
- Speed ↑ 7% / year
- ITRS* 2009 projections
  - 17 Gbits (2^{34} bits)/chip
  - 50 nm half-pitch
  - 0.8 - 1.0 V
  - $223 / chip (1st year)


System Interconnects
- Balanced architecture demands = 100s Gbytes for teraflops of computing
- Electrical based interconnects
  - Large power x volume product
  - Low performance for small message size transferred
  - Advances driven by commercial applications of network switching
- High-speed interconnects:
  - 10 Gbit Ethernet
  - 3GIO
  - HyperTransport / Infinipath
  - InfiniBand
  - Myrinet
  - QsNet
  - Rapid IO
  - SCI
  - StarFabric

*Reference: Hot Interconnects Symposium Website: www.hoti.org

System-of-Systems
Warfare in the Littoral Environment

Microprocessors
- ITRS* 2009 projections
  - Speed ↑ 60% / year
  - 773 M transistors
  - 52 nm half-pitch
  - 12 GHz clock speed
  - $85 / chip (1st year)

# Critical HPEC Enablers

## Cell Processor
- 3.2 GHz clock
- 200+ GFLOPS peak
- estimated 30-60 W

## Graphics / Video Processors
- ATI
- NVidia
- 550 MHz; 300 million transistors
- 256-512 bit memory bus
- 1-2 TOPS

## FPGAs
- Xilinx
  - 330K logic elements
  - 550 MHz clock
- Altera
  - 622 user I/O pins

## Chassis
- ATR
- VME / VME64 / VME64x
- air, conduction, or liquid cooling
- shock isolated vs. hard mounted

## Interconnects
- 10 Gbit Ethernet
- 3GIO
- HyperTransport / Infinipath
- InfiniBand
- Myrinet
- QsNet
- RapidIO
- SCI
- StarFabric

## Software
- VSIPPL / VSIPPL++
- MPI
- CORBA
- VxWorks
- Linux / RT Linux
- Service-Oriented Architecture
  - XML
  - WSDL
  - SOAP
  - UDDI
Cell Multi-Processor System

- Total peak performance over 200 GFLOPS running at 3.2 GHz
- 90 nm CMOS process
- 25.6 GBytes/sec to Rambus DRAM
- Up to 20 GBytes/sec communication bandwidth to graphics processor

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⇒ • The Next Decade and Net-Centric Architectures
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Accuracy is more Important Than Precision when Projecting Forward

“Cramming More Components Onto Integrated Circuits,” Dr. Gordon Moore
Electronics Magazine, April 19, 1965 “2x/12 months”

Prof. Carver Mead Coins the Term “Moore’s Law”

In 1975 Dr. Gordon Moore amends Original Statement to “2x/24 months”

As Progress Continued Industry Modified Original Statement to “2x/18 months”

Gordon Moore Recent Comments*:
• “You know, engineers, we’re always way too optimistic in the short run. But in the long run, it will evolve much further than we can see now.”
• “I can never see more than about three generations…. The generation now is a couple of years….So I can see six to eight years further.”

HPEC Spanning a Broader Spectrum of Application

Note: Spectrum of applications credited to Bob Graybill, DARPA PCA Program.
Changes in Force Structure*
- Navy Example -

Evolving

Today
Platform-Centric

- Stove-pipes
- Limited flexibility to adapt to new missions
- Large foot-print

Tomorrow
Network-Centric

- Network-based vs. hub and spoke model
- Global connectivity and continuous information sharing
- Expeditionary forces

* Extracted from C4ISR for Future Naval Strike Groups, National Research Council
Migrating to a Net-Centric Architecture

Global Information Sharing

Net-Centric Technologies

- **Commercial sector**
  - Service oriented architectures
  - Web services
  - Terrestrial and wireless communications
  - Semantic Web

- **Military sector**
  - Global Information Grid
    - GIG-Bandwidth Expansion (terrestrial)
    - Joint Tactical Radio System
    - Transformational Satellite (TSAT)
    - Network Centric Enterprise Services (Core enterprise services to the GIG)
    - Information Assurance (encryption)
    - Teleport (theater, reach-back)
    - Joint network management system (joint network management tools)
Building from a Commercial Service-Oriented Architecture

Commercial Enterprise

Community of Interest

Banking  Financial Industry  Travel

Service-Oriented Architecture

XML Information Format  WSDL Web Services Description  SOAP Web Services Access  UDDI Web Services Registry

Security  Messaging  Databases

Global Networks and Wireless Communications

Commercial Routers, Switches, Cell Phones, IPv6, etc.

Applications

Network Services

Physical to Transport Layer

* NCES = Net-Centric Enterprise Services
* HAIPE = High Assurance IP Encryption Hardware
* GIG = Global Information Grid
Web Services Basics*

XML: Information format
WSDL: Web services description
SOAP: Web services access
UDDI: Web services registry

Service = “A function that is well defined, self contained, and does not depend on the context or state of other services”

Building from a Commercial Service-Oriented Architecture

Commercial Enterprise

- Community of Interest
  - Banking
  - Financial Industry
  - Travel

Military Enterprise

- Community of Interest
  - Collaboration
  - Mediation
  - IA / Security

Service-Oriented Architecture

- XML Information Format
- WSDL
- SOAP
- UDDI

- Security
- Messaging
- Databases

Network Services

- Application
- Messaging
- User Assistant

Physical to Transport Layer

Global Networks and Wireless Communications

- Commercial Routers, Switches, Cell Phones, IPv6, etc.

Transformational Communications

- GIG-BE, TSAT, JTRS, HAIPE, etc.

* NCES = Net-Centric Enterprise Services
* HAIPE = High Assurance IP Encryption Hardware
* GIG = Global Information Grid
HPEC Opportunities

**Advanced HW**
- FPGAs, Standard Cell ASICs for high-performance front-end sensor processing
- Mixed circuit & custom VLSI at the sensor extreme front-end

**Programmable Processors**
- GPUs, Cell, Clearspeed, PCAs
- Rad tolerance
- Low power
- Anti-tamper

**Development Tools**
- Co-design, co-development of hybrid processors
- Model-driven architectures
- Rapid-prototyping tools

**Software**
- Runtime environments for hybrid systems
- Intelligent middleware for on-line optimization
- Middleware for GPUs, PCAs, Cell,…

**Systems**
- Smart sensors with knowledge-based processing
- Service-oriented sensors
- Collaborative HPEC in scalable networks
- Multi-function, multi-modal agility

**Hardware (CPU, Memory, I/O)**
- Operating System
- Middleware
- API
- Beam Scheduler
- External Comm.
- Console I/O
- Classifier
- Automation
- Pulse Compression
- Coherent Processing
- CFAR Detection
- Multi-Target Tracker
- Track File Maintenance
- Search/Scan
Summary

• High performance embedded computing has gone through a significant evolution over the last 15 years
  – Started as a principally a custom-based set of solutions
  – The evolution forced a more COTS-based solution
  – Meeting today’s requirements demands a hybrid solution

• The new set of conflicts (e.g. GWOT) is demanding much rapid deployment cycle
  – Enemy changes tactics too fast compared to our acquisition cycle

• The DoD landscape will continue to demand significant embedded computing capabilities
  – A wide spectrum of solutions are available ranging from programmable processors, rapidly reconfigurable FPGAs, to custom VLSI designs

• One emerging area is in distributed computing in support of net-centric architectures
  – Many TeraOps in computation
  – Distributed memory and archiving
  – Fast I/O and interconnects