Digital Beam Former Architecture

- **Sensor Interface**
  - 10 Gbit Ethernet
- **Pre-Processing Filtering**
  - Bandwidth & Equalization of each Sensor channel
- **Data Queuing**
  - Queue A/D, IQ or Beam Data to support testing and Data Recording concurrently with processing
- **Beam Forming**
  - Digitally form multiple beams for various beam patterns
- **Data Recorder**
  - High speed JBOD interface with 4 supporting Serial FPDP 2.5 Gbit interfaces
- **DSP Interface**
  - Provide elastic interface to DSP subsystem through a RapidIO network
Pre-Processing Functions

Filter Functions

- Digital Product Detector and Rate Interpolator
  - Polyphase structure rapidly cycles through coefficient phases
- Multi-channel implementation possible

A/D Samples → Digital Product Detection → Rate Interpolation → Equalization → Rate Decimation

Data Buffer → WR, RD, CTL → Input → Shift Register

Coefficient phasing

R:1 → C0, C1, ..., C_{i\in\text{last}} → Multiplexer Multiplier

Align, Accumulate & Sum
Processing Nodes

- 3 Xilinx Virtex-II Pro P70 FPGAs
- 32 MB SRAM 128 MB RLDRAM
- RapidIO Interface