Hybrid Floating point Technique yields 1.2 Giga-sample per second 32 to 2048 point floating point FFT in a single FPGA

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Apply floating point to larger functions

Barrel Shift
Denormalize

Mantissas

Exponent
Difference

Max
Exponent

Exponent
Adder

Barrel Shift
Renormalize

Fixed
point
function

Leading
Zeros
Detect

Rounding

Mantissa

Exponent

½
FFT output is only as precise as largest input

- Cascade of butterfly elements
- Each output is essentially an adder tree with phase rotators
  - Rotators don’t change scale
  - Inputs right shifted to match scale of largest input
  - Intermediate renormalizing not effective
  - Term from every FFT input
- 1 bit growth per stage
  - Renormalize maintains width
  - Alternative: grow word width
- Similar effect in other FFTs
  - Winograd, Sande-Tukey, Singleton etc.)
1.2 GSample/sec IEEE floating point FFT

Input Buffer → 32 to 2K pt floating pt FFT → Output buffer