A New Class of High Performance FFTs

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High Performance Embedded Computing (HPEC)
Workshop

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Comparative Features

- Transform size $N$ not restricted to powers of two
- Circuit is scalable
- Uses block floating point and floating point
- Higher throughput
- Low computational latency
- Based on small, simple PE (adder), locally connected
- 1-D or 2-D transforms
Performance Comparison: 256-point DFT

<table>
<thead>
<tr>
<th>Category</th>
<th>Altera</th>
<th>Base-4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Throughput (cycles/DFT)</td>
<td>256</td>
<td>240</td>
</tr>
<tr>
<td>Clock speed (MHz)</td>
<td>302</td>
<td>363</td>
</tr>
<tr>
<td>Throughput (µsec)</td>
<td>0.85</td>
<td>0.67</td>
</tr>
<tr>
<td>Signal/Noise (db)</td>
<td>86.9</td>
<td>89.0</td>
</tr>
<tr>
<td>Total ALUTs</td>
<td>7555</td>
<td>7790</td>
</tr>
<tr>
<td>18-bit multipliers</td>
<td>12</td>
<td>16</td>
</tr>
</tbody>
</table>

![Multiplier Diagram]

**Multipliers**
- Adder Array 1
- Adder Array 2

**Connections**
- Input Data (X)
- Coefficient