Panel Session: 
*Looking Forward, Looking Back*

James C. Anderson  
MIT Lincoln Laboratory  
HPEC06  
Wednesday, 20 September 2006

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Objective & Schedule

- **Objective:** using lessons learned from the last 10 yrs, project the next 10 yrs of HPEC technology & its impact on DoD systems

- **Schedule**
  - 1540-1600: Overview
  - 1600-1605: Introduction of the panelists
  - 1605-1620: Guest speaker Steve Poole
  - 1620-1700: Previously-submitted questions for the panel
  - 1700-1725: Open forum
  - 1725-1730: Conclusions & the way ahead
Looking Forward, Looking Back

How can we hope to make relevant analyses & projections over such a time span?

Bust of the Roman god Janus

10 yrs into the past & future, or 2006 ± ½%

20 min to cover 20 yrs, or 1% of time since ancient Rome!
It Doesn’t Get Any Better Than This

• 1995: smallest hearing aid battery
  – So tiny that a dozen easily fit in volume of a U.S. nickel
  – Not likely to get any smaller (too difficult for elderly to handle)

• 1996: automotive toll-collection transponders
  – Prototype systems developed by many major manufacturers (including Digital Equipment Corp., Raytheon & Texas Instruments)
  – No further improvements req’d after specs met
    # of vehicles @ given speed in operating zone
    Xpndr frequency, size, power, lifetime & reliability

• 2002: analog-to-digital converters for audio market
  – 24-bit resolution (18 effective bits) & 40 KHz analog bandwidth
  – Approaches or exceeds limits of human hearing
  – Future improvements likely limited by thermal noise

Some problems get “solved,” and improvement rates may level off after key requirements are met
Highest-performance COTS (commercial off-the-shelf) ADCs (analog-to-digital converters), 1Q06

*Performance limiters shown are “design challenges” rather than “hard limits” (R.H. Walden, IEEE Jour. on Selected Areas in Comm., Apr. 1999)
Moore is Less

- "Original" Moore’s Law (1965, revised 1975): 4X transistors/chip every 3 yrs
- Improvements came from decreasing geometry, increasing chip size & "circuit cleverness"
- Held from late ’70s - late ’90s for memory chips

Slide #12 from Gordon Moore’s “No Exponential is Forever … but We Can Delay ‘Forever’,” ISSCC03, www.intel.com/technology/silicon/mooreslaw

Pre-Y2K improvement rate was faster (lithography improved frequently & chip size grew)
Hardware Improvement Rate Has Slowed in the Last Decade

- 1997 Edition of the *National Technology Roadmap for Semiconductors* (NTRS97) projected µP improvements @ 4.7X every 3 yrs
  - 2.8X density (transistors/area)
  - 1.2X chip size growth (300 mm² size in 1997 to 750 mm² in 2012)
  - 1.4X speed @ constant power

- 2005 Edition of the *International Technology Roadmap for Semiconductors* (ITRS05) projects µP improvements @ 3.2X every 3 yrs (for FPGAs, ASICs & multi-core processors)
  - 2X density (limited by lithography improvement rate & partially driven by economics)
  - No chip size growth
    - Growth ceased ~1998
    - µP chip size @ 310 mm² or less through 2020
  - 1.6X speed @ constant power

- At present, improvements for general-purpose uni-processors with large on-chip cache may be limited to 2X every 3 yrs

Latest projected improvement rate is still substantial, even if Improvement = 2^{Years/3}
Microprocessor Family Improvement Rate Model

- Derived from ITRS05 projections
  - $1/\sqrt{2}$ geometry reduction every 3 yrs
  - Constant chip size & power

- Next-generation dual-core chip
  - 3X performance (2X transistors @ 1.5X speed, but 1/3 fewer bytes/OPS*)
  - Incompatible HW/SW (2X pins, not a uni-processor)

- Next-generation uni-processor
  - 2X performance (2X transistors @ same speed, bytes/OPS* unchanged)
  - Compatible HW/SW

- Present-generation uni-processor

*Operations per second, or “throughput”
Timeline for Highest Performance COTS Multiprocessor Card Technologies, 3Q06

Card-level I&O complex sample rate sustained for 32 bit flt-pt 1K complex FFT (1024 MSPS for FFT computed in 1μs with 51.2 GFLOPS) using 6U form factor convection-cooled cards <55W

Open systems architecture goal: mix old & new general- & special-purpose cards, with upgrades as needed (from 1993-2003, a new card could replace four 3-yr-old cards)
Improvements in COTS Embedded Multiprocessor Card Technologies, 3Q06

General-purpose RISC (with on-chip vector processor) cards (~10 FLOPS/byte) improving 2X in 3 yrs

Reconfigurable FPGA cards (~100 FLOPS/byte) improving 3X in 3 yrs

70 W/Liter convection cooling limit

Similar performance pre-Y2K

Special-purpose ASIC cards (~10 FLOPS/byte) improving 3X in 3 yrs

Projected 2010 performance gap due to different improvement rates
The Decades Beyond *Deep Blue*

- **5/97:** *Deep Blue* beats chess champ Kasparov
  - Custom ASICs
  - Comparable to a computer with up to 40 trillion operations per second
  - 1270 kg

- **10/02:** *Deep Fritz* ties chess champ Kramnik

- **1-2/03:** *Deep Junior* ties former champ Kasparov

  - *Deep Fritz* & *Deep Junior* are programs running on general-purpose servers
    - ~10,000 lines of C++
    - 15 billion instructions per second & 3 billion bytes of memory (5 IPS/byte)
Food for Thought

- Feasible ~2005
- **Deep Dew** hand-held chess champ
  - 0.6 L & 0.6 kg
  - 22W for 3.5 hrs (22 AA Li/FeS$_2$ cells)
  - COTS devices include voice recognition & response chip for I/O
More Food for Thought

• Feasible ~2005
• *Deep Dew* hand-held chess champ
  – 0.6 L & 0.6 kg
  – 22W for 3.5 hrs (22 AA Li/FeS$_2$ cells)
  – COTS devices include voice recognition & response chip for I/O

• 2008: *Deep Yogurt* based on improved *Deep Dew* design
  – 1/3 the size & power
  – 3X improvement in 3 yrs
Still More Food for Thought

• Feasible ~2005
• Deep Dew hand-held chess champ
  – 0.6 L & 0.6 kg
  – 22W for 3.5 hrs (22 AA Li/FeS₂ cells)
  – COTS devices include voice recognition & response chip for I/O

• 2008: Deep Yogurt based on improved Deep Dew design
  – 1/3 the size & power
  – 3X improvement in 3 yrs

• 2015: Deep Fried has challenging weight & form factor constraints
  – I/O via accelerometer & vibrating motor
  – Unaided hens already beat humans at tic-tac-toe
Power per Unit Volume (Watts/Liter) for Representative Systems, 2002-2015

- **2002:** Deep Fritz & Deep Junior Chess Server
- **2005:** Deep Dew (or soldier’s radio)
- **2008:** Deep Yogurt (or processor for small UAV)
- **2015:** Deep Fried (or robot controller)

Throughput in GIPS (billions of Dhrystone instructions/sec)

- 1000 W conduction cooling limit
- 70 W convection cooling limit
- 1.6 W moderately active human (human vs. machine “Turing Tests”)

- Packaging & integration (system-on-chip)
- Algorithms & SW
- Improvement drivers
- Semiconductor process

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Looking Forward, Looking Back

Panelists

- Dr. James C. Anderson, MIT Lincoln Laboratory (moderator)
- Mr. Jerry Oesterheld, SimVentions
- Mr. Richard Ridgley, National Reconnaissance Office
- Dr. Gary Shaw, MIT Lincoln Laboratory
- Mr. Stephen Poole, Oak Ridge National Laboratory & Los Alamos National Laboratory

Panel members & audience may hold diverse, evolving opinions
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Conclusions & The Way Ahead

• In areas where many problems have been “solved” during the last decade, little progress is expected during the next decade

• Although there has been an improvement rate slowdown vs. historical Moore’s Law, the rate is still substantial

• Due to the slowdown, advanced packaging technology has increased importance in applications requiring high computation density

The coming decade will see applications that are not yet on anybody’s drawing boards!
### NTRS97

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<thead>
<tr>
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</thead>
<tbody>
<tr>
<td><strong>Year of 1st product</strong></td>
<td></td>
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<td></td>
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<tr>
<td><strong>shipment</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>DRAM half-pitch, nm</strong></td>
<td>250</td>
<td>130</td>
<td>100</td>
<td>70</td>
<td>50</td>
</tr>
<tr>
<td><strong>Mbits per sq cm</strong></td>
<td>96</td>
<td>770</td>
<td>2200</td>
<td>6100</td>
<td>17,000</td>
</tr>
<tr>
<td><strong>Allowable max pwr,</strong></td>
<td>70</td>
<td>130</td>
<td>160</td>
<td>170</td>
<td>175</td>
</tr>
<tr>
<td><strong>high-performance,</strong></td>
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<td><strong>W</strong></td>
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<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>On-chip clock, MHz</strong></td>
<td>750</td>
<td>2100</td>
<td>3500</td>
<td>6000</td>
<td>10,000</td>
</tr>
<tr>
<td><strong>Clock freq, MHz, for</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>70W power</strong></td>
<td>750</td>
<td>1131</td>
<td>1531</td>
<td>2471</td>
<td>4000</td>
</tr>
<tr>
<td><strong>Chip size (mm²)</strong></td>
<td>300</td>
<td>430</td>
<td>520</td>
<td>620</td>
<td>750</td>
</tr>
<tr>
<td><strong>Max improvement:</strong></td>
<td></td>
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<td></td>
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<td><strong>density x size x</strong></td>
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<td></td>
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<tr>
<td><strong>speed@70W</strong></td>
<td></td>
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<td></td>
</tr>
</tbody>
</table>

### ITRS05

<table>
<thead>
<tr>
<th></th>
<th>2006</th>
<th>2009</th>
<th>2012</th>
<th>2015</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Year of production</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>DRAM half-pitch, nm</strong></td>
<td>70</td>
<td>50</td>
<td>36</td>
<td>25</td>
</tr>
<tr>
<td><strong>Mxstrs per sq cm</strong></td>
<td>283</td>
<td>566</td>
<td>1133</td>
<td>2265</td>
</tr>
<tr>
<td><strong>Allowable max pwr,</strong></td>
<td>180</td>
<td>198</td>
<td>198</td>
<td>198</td>
</tr>
<tr>
<td><strong>high-performance,</strong></td>
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<td><strong>W</strong></td>
<td></td>
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</tr>
<tr>
<td><strong>On-chip clock, MHz</strong></td>
<td>6783</td>
<td>12,369</td>
<td>20,065</td>
<td>33,403</td>
</tr>
<tr>
<td><strong>Clock freq, MHz, for</strong></td>
<td></td>
<td></td>
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<tr>
<td><strong>70W power</strong></td>
<td>2638</td>
<td>4373</td>
<td>7094</td>
<td>11,810</td>
</tr>
<tr>
<td><strong>Chip size (mm²)</strong></td>
<td>195</td>
<td>195</td>
<td>195</td>
<td>195</td>
</tr>
<tr>
<td><strong>Max improvement:</strong></td>
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<td><strong>density x size x</strong></td>
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<td><strong>speed@70W</strong></td>
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Representative 90nm Devices ca. 2006

- **µP: Freescale MPC7448 PowerPC**
  - 10W @ 1.4 GHz
  - 11.2 GFLOPS peak (1.1 GFLOPS/W peak for chip alone), single-precision
  - 1088 Kbytes on-chip memory (10K FLOPS/byte)

- **IBM Cell Broadband Engine**
  - 100W (est.) @ 3.0 GHz
  - 192 GFLOPS peak (1.9 GFLOPS/W peak, est., for chip alone), single-precision
  - 2592 Kbytes on-chip memory (74K FLOPS/byte)

- **FPGA: Xilinx Virtex-4 LX200**
  - 54W (est.) @ 225 MHz core & 375 MHz I/O (2 devices with external memory & I/O on 6U card)
  - 51.2 GFLOPS sustained (0.95 GFLOPS/W sustained, est., for complete card), single-precision
  - 528 Mbytes DDR-SRAM on card (97 FLOPS/byte)

Although Cell has greater computation efficiency (operations per watt), PowerPC has more on-chip memory for a given throughput
Representative COTS Primary (non-rechargeable) Cells

<table>
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<tr>
<th>Type</th>
<th>Chemistry</th>
<th>Nominal/cutoff voltage (volts)</th>
<th>Nominal energy (watt-hours)</th>
<th>Weight (grams)</th>
<th>Gravimetric energy density (Wh/kg)</th>
<th>Volume (cubic cm)</th>
<th>Volumetric energy density (Wh/Liter)</th>
<th>High-drain capability (constant power)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Zinc air 675-size (non-stackable) hearing aid</td>
<td>Zinc air (Zn/O₂)</td>
<td>1.4/1.1</td>
<td>0.66</td>
<td>1.85</td>
<td>357</td>
<td>0.57</td>
<td>1150</td>
<td>Poor: 15 mW max. (12 mA limiting current)</td>
</tr>
<tr>
<td>Alkaline C-size flashlight</td>
<td>Zinc manganese dioxide (Zn/MnO₂)</td>
<td>1.5/0.8</td>
<td>8.3</td>
<td>64</td>
<td>131</td>
<td>26</td>
<td>323</td>
<td>Good: 1W for 3.6 hrs (0.324Ω internal resistance when fresh)</td>
</tr>
<tr>
<td>Lithium AAA-size (AA-size) digital camera</td>
<td>Lithium iron disulfide (Li/FeS₂)</td>
<td>1.5/1.0</td>
<td>1.5</td>
<td>7.6</td>
<td>200</td>
<td>3.8</td>
<td>400 (453)</td>
<td>Good: 0.5W (1W) for 3 (3.6) hrs w/ 2A limiting current</td>
</tr>
</tbody>
</table>

Zinc air has high energy density but limited current, alkaline has lowest cost, lithium has best performance (& low self-heating) for high-drain applications.
ADC Database (printable notes page) for “Highest-performance COTS (commercial off-the-shelf) ADCs (analog-to-digital converters), 1Q06”

James C. Anderson, JCA@LL.MIT.EDU, 1/6/06; non-proprietary vendor data from analog-to-digital converter historical database dated 1/6/06.

When a value for the effective number of bits (ENOB) has not been provided by the manufacturer, one has been calculated using the approximation ENOB = (SINAD – 1.76)/6.02, where SINAD is the signal to noise-and-distortion ratio (typically expressed in dB relative to a nearly full-scale sine wave input having a frequency nearly half the sampling rate). Energy required for each effective quantization level is EQ=Power/[2**(ENOB) x (sampling rate)], and includes on-chip de-multiplexer if any.

1986-1990:
10 MSPS 14-bit (ENOB=12.0) 10/90 Analog Devices AD9014, SINAD=74dB, SFDR=87dB, 12.8W, EQ=310pJ; 2 ECL hybrid DIPS on small PCB
50 MSPS 10-bit (ENOB=9.3) 10/88 SPT (Honeywell) HADC77600, SINAD=58dB, SFDR unknown, 4.7W, EQ=150pJ; 1.2um bipolar monolithic flash
500 MSPS 8-bit (ENOB=6.8) 1/89 Tektronix TKAD10C, SINAD=42.7dB, SFDR unknown, 7.5W, EQ=130pJ; hybrid DIP, 1:2 DMUX (250 MSPS matched ping-pong)

1991-1995:
400 KSPS 16-bit (ENOB=14.8) 7/92 Analog Devices AD1382, SINAD=91dB, SFDR=85dB, 12.8W, EQ=250pJ; hybrid DIP, 500 KSPS max.
5.12 MSPS 14-bit (ENOB=12.7) 11/92 Burr-Brown ADC614LH, SINAD=78dB, SFDR unknown, 4.7W, EQ=150pJ; ECL hybrid DIP
41 MSPS 12-bit (ENOB=10.8) 4/95 Analog Devices AD9042, SINAD=67dB, SFDR=80dB, 0.6W, EQ=8pJ; high-speed complementary bipolar (XCFB)

1996-2000:
80 KSPS 24-bit (ENOB=16.8) 4/00 AKM AK5393, SINAD=103dB, SFDR=117dB, 0.47W, EQ=16; 2-ch delta-sigma with on-chip filters & 96 KSPS output
2 MSPS 16-bit (ENOB=13.7) 11/98 Analog Devices AD9260, SINAD=84.5dB, SFDR=105dB, 0.61W, EQ=22pJ; CMOS, 20 MHz clock & 2.5 MSPS output
65 MSPS 14-bit (ENOB=11.8) 10/99 Analog Devices AD6644, SINAD=73dB, SFDR=85dB, 1.3W, EQ=5.6; high-speed complementary bipolar (XCFB)
105 MSPS 12-bit (ENOB=10.9) 3/99 Analog Devices AD9432-105, SINAD=66.7dB, SFDR=80dB, 0.85W, EQ=4.2; BiCMOS
210 MSPS 10-bit (ENOB=8.6) 10/00 Analog Devices AD9410, SINAD=52.5dB, SFDR=58dB, 2.1W, EQ=26pJ; BiCMOS, 1:2 DMUX
1 GSPS 8-bit (ENOB=7.55) 5/00 Maxim MAX104, SINAD=46.2dB, SFDR=54.1dB, 3.3W, EQ=19; bipolar, 1:2 DMUX
2 GSPS 8-bit (ENOB=4.3) 3/98 Rockwell RSC-ADC800, SINAD=27.5dB, SFDR=30dB, 5W, EQ=130pJ; bipolar, Gray code output

2001-2005:
80 KSPS 24-bit (ENOB=18.0) 7/02 AKM AK5394A, SINAD=110dB, SFDR=120dB, 0.67W, EQ=16; 2-ch delta-sigma with on-chip filters & 96 KSPS output
160 KSPS 24-bit (ENOB=15.3) 7/02 AKM AK5394A, SINAD=94dB, SFDR=100dB, 0.67W, EQ=52; 2-ch delta-sigma with on-chip filters & 192 KSPS output
80 MSPS 16-bit (ENOB=12.9) 12/03 Analog Devices AD10678, SINAD=79.7dB, SFDR=94.2dB, 6.9W, EQ=11pJ; PCB w/ quad 14-bit ADCs & digital post-processing
100 MSPS 16-bit (ENOB=12.8) 12/05 Analog Devices AD9446-100, SINAD=78dB, SFDR=89dB, 3.6W, EQ=3.6pJ

(up to 0.5 bit/octave processing gain could provide 5 additional bits, for ENOB=17.8, at a 97.7 KSPS effective sampling rate)

105 MSPS 12-bit (ENOB=10.5) 7/03 Analog Devices AD9430-210, SINAD=64.5dB, SFDR=77dB, 1.3W, EQ=4.3pJ; BiCMOS, 1:2 DMUX
400 MSPS 12-bit (ENOB=9.8) 3/03 Analog Devices AD12400, SINAD=61dB, SFDR=71dB, 7W, EQ=19pJ; module w/ dual 12-bit ADCs & digital post-processing

Performance limiters based on selected values from Fig. 7 of Robert H. Walden’s “Analog-to-Digital Converter Survey and Analysis,” IEEE Journal on Selected Areas in Communications, Vol. 17, No. 4, April 1999, pp. 539-550. These should be considered as “design challenges” rather than “hard limits.” For example, the thermal noise can be reduced by reducing the effective resistance or temperature, but at additional cost.

Thermal noise (2000 ohms): 17.8 bits @ 0.1 MSPS & 12.5 bits @ 100 MSPS for 5.3 bits drop-off in 3 decades = 10 octaves. Verification: this curve matches the max. processing gain with linearization curve for the AD9446-100, which is another way to effectively “create” an ADC having lower sampling rate.

Aperture uncertainty (0.2 ps): 13 bits @ 100 MSPS & 8.5 bits @ 2.3 GSPS for 4.5 bits drop-off in ~4.5 octaves. Verification: LTC2208 (ENOB=12.6 @ 130 MSPS) vs. Agilent Infinium DSO80000 (ENOB=4.6 @ 6 GHz & 20 GSPS, with equivalent sampling rate = 12 GSPS) gives 8 bits in ~7 octaves, and this result is consistent with Rockwell Scientific RAD006 (ENOB=5.5 @ 6 GSPS).