World’s First Polymorphic Computer – MONARCH

- System on a Chip
  - 64 GFLOPS
  - 12 MBytes RAM
  - 43 GBytes/s I/O rate
  - Memory BW
    - on chip >60 GBytes/s
    - off-chip >10 GBytes/s
- Power sustained 5 GFLOPS/W
- Standard interfaces
  - Serial Rapid IO – 2 ports
  - DDR2 – 2 ports
- Key physical characteristics
  - 18.76 mm X 18.76 mm
  - 1.5 Km wiring
  - 280 Million cells

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MONARCH Silicon is here TODAY!

First Pass Functional Silicon
What is MONARCH?
MOrphable Networked micro-ARCHitecture

- Single, programmable chip type which can replace custom ASICs
  - Saves $20-30M development cost and 18-36 months of development schedule per ASIC
- Processing throughput of 10 Pentiums
- Power and performance similar to custom ASICs >3 GFLOPS/W
- Programmable and Scaleable
- Balanced I/O & Processing uniquely suited to Signal Processing needs

System-on-a-Chip:
Standalone solution for embedded applications
Enabler for ultra small UAVs, hand-holds, munitions, etc.

GPS SDR
Current anti-jam implementation...
- 1 Custom ASIC
- 2 Vertex II Pro FPGAs
- TMS-320 µP
- Flash Memory
- RAM

...Replaced by a single MONARCH chip!
Provides completely programmable solution
Potential for future algorithm upgrades

Tiled Array: TFLOP performance in a self-contained network
Enabler for embedded advanced, adaptive signal processing

MONARCH board provides >5x improvement in processing throughput, weight, and power for Global Hawk
Monarch Chip Overview

- 6 RISC Processors
- 12 MBytes on-chip DRAM
- 2 DDR-2 External Memory Interfaces (8 GB/s BW)
- Flash Port
- 2 Serial RapidIO Interface
- 16 IFL ports (2.6 GB/s ea)
- On-chip Ring 40 GB/s
- Reconfigurable Array – FPCA (64 GFLOPS)
MONARCH Architecture

Features

◆ Dual native mode, high throughput computing
  – Multiple wide word threaded (instruction flow) processors/chip
  – Highly parallel reconfigurable (data flow) processor

◆ Flexible on-chip memories
  – Multiport memory clusters
  – High bandwidth access to EDRAM
  – Extensible with off chip memory

◆ High speed, distributed cross bar I/O
  – Integrated with chip processing
  – Scalable I/O bandwidth - multiple topologies
  – Direct connect to high speed I/O devices, e.g., A/D’s

◆ Rich on chip interconnect
  – Supports on chip topology morphing and fault tolerance
  – Supports multiple computation models (SISD, SIMD, DF, SPMD,...)

◆ On chip Morph - Program bus and microcontrollers
Computation Attributes

◆ Fixed point arithmetic
  – 8, 16, 32, and 40 bit arithmetic
  – Signed, unsigned, saturating modes

◆ Floating point arithmetic
  – 32 bit IEEE formats

◆ SIMD and data flow control
  – 256 bit SIMD data path (8 to 32 parallel ops)
  – >256 data flow elements per chip

◆ In streaming mode, data tokens accompany each data element
  – 2 bit field
  – Used for end of stream and other function control
FPCA – Basic Paradigm

- FPCA contains multiple compute and memory resources within an interconnect fabric
- Static mapping of “operation” to H/W element (ALU/Multiplier/Memory)
- Distributed control (no central “controller”)
- Dynamic/data dependent operations supported
MONARCH – Physical Design

- Standard cell ASIC
- 90 nm bulk CMOS
- 18.76mm x 18.76mm
- 280 million cells
- 10.5 million nets
- Over 1.5 km wire!!
- 1059 signal I/O
- 333 MHz
- 31-42W
- Tape out Oct 10, 2006
- First silicon Dec 22
MONARCH Chip Test Environment

- Drive or loop-back all interfaces
- Modify voltage and clock frequency
- Monitor voltage, current and temperature
- Identical S/W environment to Emulator
FIR Filter Details

- FIR filter implemented using direct-form 2
  
  ![FIR Filter Diagram]

- Directly maps to FPCA
- 96 Tap FIR Filter uses all 96 floating point adders and all 96 floating point multipliers
- Sustains full 333 MSamples/s giving 64 GFLOPS!
- Can also insert FIFOs to use all 124 memory elements (248 address generators)
GFLOPS per Watt (FIR) Versus Process and Voltage

- **64 GFLOPS FIR Filter (no I/O, no FIFOs)**

<table>
<thead>
<tr>
<th></th>
<th>Low VDD (0.95v)</th>
<th>Nominal VDD (1.25V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Faster Part</td>
<td>5.8 GFLOPS/W (10.9W)</td>
<td>3.1 GFLOPS/W (20.9W)</td>
</tr>
<tr>
<td>(158ns PSRO)</td>
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<tr>
<td>Nominal Part</td>
<td>6.6 GFLOPS/W (9.6W)</td>
<td>4.1 GFLOPS/W (15.6W)</td>
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<td>(195ns PSRO)</td>
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NOTE: The low Vdd operating condition is outside the chip design parameters
FFT Implementation

- Input/Output: A = samples 0 to n/2-1, B = samples n/2 to n-1.
- For larger FFTs (512 to 2K), early stages and bit reverse need more MCs
- 16 point uses 4 ACs – 3 instances can be mapped per FPCA
- 2K point uses 11 ACs (maximum size due to extra MCs required)
MONARCH FFT Performance

MONARCH FFT Benchmark

- **MONARCH Notes…**
  - For $N \leq 2048$
    - Radix-2 implementation
    - $N=16$ and $N=2K$ verified on chip
  - For $N > 2048$
    - Mixed-radix implementation
    - Performance is estimated, Currently being mapped and coded

- **Pentium Notes…**
  - Benchmark values gathered from FFTW web site
  - <http://www.fftw.org/speed/Pentium4-3.60GHz-icc/>

34 GFLOPS (3 per FPCA)

31.2 GFLOPS
GFLOPS per Watt (FFT) Versus Process and Voltage

- 2K Point FFT (31.2GFLOPS) (no I/O)
- For comparison IBM Cell is 0.5 GFLOP/W

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<tr>
<td>Faster Part</td>
<td>1.8 GFLOPS/W (17.6W)</td>
<td>1.3 GFLOPS/W (23.3W)</td>
</tr>
<tr>
<td>(158ns PSRO)</td>
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<td></td>
</tr>
<tr>
<td>Nominal Part</td>
<td>2.9 GFLOPS/S (10.7W)</td>
<td>2.6 GFLOPS/W (12.1W)</td>
</tr>
<tr>
<td>(195ns PSRO)</td>
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NOTE: The low Vdd operating condition is outside the chip design parameters
MONARCH Power Measurements (Reduced Core Voltage, Nominal Part)

- **32W – 33W**
  - **7.1W**
  - **2.8W**
  - **8.3W**
  - **0.7W**
  - **1.3W**
  - **0.6W**
  - **4.1W**
  - **4.4W**
  - **2.3W to 3.2W**

**External Memory – Dual Port 3.3 GB/s each**
(MMBT write test)

**4 IFLL High speed I/O (2.6 GB/s)**
(IFLL bit error rate test)

**12 IFLH High speed I/O (2.6 GB/s)**
(IFLH bit error rate test)

**System I/O – Dual Rapid IO (estimate)**
All MMBT 13.3 (GB/s)
All RISCs (2 GOPS)
All computing & memory elements 64 GFLOPS

**Clocks, EDRAM refresh & infrastructure, Bi-Directional I/Os disabled**

**Leakage (30C to 70C)**

**64 GFLOPS – Off chip**

**6.7W**

**11.0W**

**2.3W to 3.2W**

**Standby**

**64 GFLOPS – On-chip**

**NOTE:** The low Vdd operating condition is outside the chip design parameters
MONARCH SW Tools

◆ RISC C/C++ compiler
  – Validated C++ compiler from Code Sourcery
  – Automatic vectorization for wide word (limited testing)
  – Supports gcc vector data types for the Wide Word processors

◆ RISC assembler

◆ RISC Operating System
  – RTEMS
  – Real-time, Embedded
  – Not validated on chip

◆ RISC Libraries
  – VSIPL Core Plus and SAL (for a single processor)

◆ FPCA Libraries
  – Signal processing routines (FFT, FIR)

◆ FPCA tools
  – Assembler, Router

◆ Simulator
  – Simulate FPCA and RISC
  – Gdb debugging for RISC programs
Looking to the Future

- Improved software tools are essential
- Performance per Watt
- Lower total power
- Security/AT/Crypto
- Improved SWEPT for mission level enablers

<table>
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<tr>
<th>90 nm respin</th>
<th>45 nm respin with minimal mods</th>
<th>45 nm respin with larger mods</th>
</tr>
</thead>
</table>
| Minor Errata Fix | Leave chip design largely as is  
- New physical design  
- Update IOs as needed  
- Update architecture paths  
- Performance per Watt 4X  
- Total performance 2X | Use 3D physical design and wafer scale  
Plus those to left  
Performance per Watt >4X  
Functionality/memory growth  
Total performance >2X |

SWEPT

Size  Weight  Energy  Performance  Time
MONARCH Achieves DARPA Goals:
Meets multi mission, multi sensor,
high-efficiency processing with a
single chip type

Sensors:  
- Radar  
- SIGINT  
- Com  
- EO/IR

Functions:  
- Conditioning  
- Beamforming  
- Data creation  
- Track  
- Compression

Replaces:  
- ASIC  
- FPGA  
- DSP  
- PPC

Polymorphous Computing Architecture Program
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