Focus 3: Cell

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Embedded Processor Evolution

- 20 years of exponential growth in FLOPS / W
- Requires switching architectures every ~5 years
- Cell Processor is current high performance architecture
Cell Features

Element Interconnect Bus
- 4 ring buses
- Each ring 16 bytes wide
- Max bandwidth 96 bytes / cycle (204.8 GB/s @ 3.2 GHz)

Synergistic Processing Element
- 128 SIMD Registers, 128 bits wide
- Dual issue instructions

Local Store
- 256 KB Flat memory
- Built in DMA Engine

Memory Flow Controller

Element Interconnect Bus (EIB)

Overall Performance
- Peak FLOPS @ 3.2 GHz: 204.8 GFLOPS (single), 14.6 GFLOPS (double)
- Processor to Memory bandwidth: 25.6 GB/s
- Power usage: ~100 W (estimated)
- Cell gives ~2 GFLOPS / W

Cell offers significant performance benefits over other programmable technologies
In This Session

• FFTC: Fastest Fourier Transform for the IBM Cell Broadband Engine
  – Virat Agarwal, Georgia Institute of Technology

• Implementation of SIGINT Application on Cell-BE
  – Richard Besler, Black River Systems Company

• Performance of a Multicore Matrix Multiplication Library
  – Robert Cooper, Mercury Computer Systems
Other Cell Related Talks

**Wednesday:**
- Session 4: Novel Applications
  - Projective Transform on Cell: A Case Study

**Thursday:**
- Session 5: Multicore Environments
  - High Performance Simulations of Electrochemical Models on the Cell Broadband Engine
  - Sourcery VSIP++ for the Cell/B.E.
  - Programming Examples that Expose Efficiency Issues for the Cell Broadband Engine Architecture
  - PVTOL: A High-Level Signal Processing Library for Multicore Processors
- Focus 5: Benchmarking
  - Exploring Multi-core Processors with Realistic Signal- and Image-processing Application Benchmarks
- Poster / Demo C: Cell / GPU Technologies
- Session 6: Awards Session
  - Implementation of Polar Format SAT Image Formation on the Cell Broadband Engine