Evaluating Partial Reconfiguration for Embedded FPGA Applications

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**Baseline Architecture #1**

- Pros
  - Most flexible
  - Simplest module development with highest performance
  - Configuration controller can be radiation-hardened
  - 100% of user FPGA logic/routing resources available
- Cons
  - Highest communication bandwidth
  - State information not maintained
  - Longest reconfiguration time
  - SelectMAP pins usually no longer usable as general purpose I/O
  - Higher power/PCB requirements
  - More points of failure

- Pros
  - Lower communication bandwidth
  - Possible to maintain state information
  - Unrelated processing can continue uninterrupted during partial reconfiguration
  - Shorter reconfiguration times
  - Lower power/PCB requirements
- Cons
  - Less than 100% of logic/routing resources available
  - High overhead
  - Radiation susceptibility if COTS
  - More difficult module development
  - Varying degrees of flexibility (always lower than non-PR baseline)

**Architecture #1**

- Pros
  - 1 single region of maximal size
  - Has exclusive access to all I/O not used by static region
  - I/O type is reconfigurable
- Cons
  - No maintenance of state information
  - Highest PR bandwidth
  - Least amenable to current Xilinx toolset

**Architecture #2**

- Pros
  - Conceptually simplest – only one PRR
  - Lowest overhead
  - Least performance degradation
  - Easiest development framework
- Cons
  - Unrelated processing can continue uninterrupted during partial reconfiguration
  - Partial reconfiguration
  - Partial maintenance of state information
  - More performance degradation

**Architecture #3**

- Pros
  - Maintenance of module state information
  - Lowest PR bandwidth
  - More amenable to current Xilinx toolset
  - No maintenance of state information
  - Higher overhead
- Cons
  - Conceptually most difficult – 7 PRRs
  - Must partition I/O and communication using a best guess at design-time

**Region 1**

- Usage
  - 8320
  - XC4VLX25 Utilization: 77.4%
- Static Controller
  - Usage: 1910
  - XC4VLX25 Utilization: 17.8%
- Bus Macro Overhead
  - Usage: 522
  - XC4VLX25 Utilization: 4.9%

**Region 2**

- Usage
  - 1536
  - XC4VLX25 Utilization: 14.3%
- Static Controller
  - Usage: 1664
  - XC4VLX25 Utilization: 15.5%
- Bus Macro Overhead
  - Usage: 792
  - XC4VLX25 Utilization: 7.4%
- Wiring
  - Usage: 296
  - XC4VLX25 Utilization: 2.8%