Octopus: A Multi-core implementation

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HPEC 2007, MIT, Lincoln Lab

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Parameters to evaluate?

- **Many vendors have multi-core, multi-chip boards**

- **Characteristics of good evaluation**
  - How much memory BW among multiple cores? (i.e. core to core)
  - How much I/O BW between multiple sockets/chips on same board? (i.e. chip to chip on same board)
  - How much fabric BW across boards? (i.e. board to board)

- **CPU performance with I/O combined**
  - Data has to come from somewhere and go into memory
• **Current Benchmarks**
  - Most don’t involve any I/O
  - Many are cache centric
  - Many are single core centric (no multi-threading)

• **Questions to ask?**
  - Interrupt handling among multiple cores
  - Inter-process communication
  - How many channels for DDR2 interface? 4 or better?
  - Size, Weight and Power (SWaP) when fully loaded?
  - How to debug multi-threaded programs? Cost of tools?
  - What is the cost of ccNUMA or NUMA? Memory R/W latency?
• Single entry point for memory access
• All external I/O via Southbridge
  - GigE, UART competes with Fabric
  - Always requires CPU cycles
• Local memory access
• Mostly no I/O
• RapidIO (parallel or serial) switching
• Limited BW between chips
• Fabric bottleneck as all data comes via fabric only
DRS Approach

DRS's MIPS based Multi-socket System

- Each System on Chip (SoC) has HyperTransport switch
- Local memory access with NUMA and ccNUMA capability
- Data can come locally or via fabric

Zero CPU & memory cycles switching from any-to-any SoC
BCM1480 Architecture Overview

4-Issue SuperScalar
MIPS64 SB-1
(8 GFLOPS/Core)

Remote Memory Requests & ccNUMA Protocol

On-Chip Switch, 256 Gbps bandwidth, 5-ports

19.2 Gbps in each direction

Memory Bridge

X

Packet DMA

SoC I/O:
- 4 GigE
- 64b PCI-X
- System I/O

Multi-Channel Packet DMA Engine

102 Gbps Memory Controller

ZBbus, Split Transaction, Coherent, 128 Gbps
Performance measurement

• **How do you measure performance of multi-core embedded system?**
  - Perform network I/O while doing number crunching
    - Examples uBench, netPerf with FFTw
  - Measure memory BW with streams benchmark
  - Measure intra-core and inter SoC BW performance
    - Examples openMPI (measures latency and BW)
  - How open standards are supported?
    - Examples CORBA, VSIPL, FFTw, RDMA, MPI etc.
  - Measure switch fabric BW and latency
  - XMC and PMC plug ability and their interface speed
  - Boot time (in seconds)
### VSIPL Benchmarks

**VSIPL Comparisons**

**FFT Routines; Large Vectors**

Times in microseconds

<table>
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<th>vsip_ccfftop_f:</th>
<th>1480: 1GHz MIPS64</th>
<th>G4: 1GHz 7447</th>
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<td>N</td>
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**Performance Improvement**

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<th>1.48</th>
<th>5.05</th>
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Octopus as the Open Source/Standard and COTS commodity Solution

• Leverages open source development & run time environments
  - Including Linux OS (SMP), Eclipse IDE, GNU tools
  - Promotes ease of portability and optimal resource utilization

• Delivers open standard middleware & signal processing libraries
  - Including VSIPL, MPI, FFTw and CORBA

• Effectively decouples the application software from the hardware
  - Applications interface to the OS at a high level (layer 4)

• Utilizes standards based hardware
  - VITA 41 (VXS) backplane – backwards compatible with VME
  - VITA 42 (XMC) mezzanine standards - permits rapid insertion of new technology

• Implemented using commodity chips taken from large adjacent markets
  - Broadcom dual/quad core processors from Telecom/Datacom Network Processing
  - HyperTransport from commodity computing
  - Dune fabric from the Tera-bit router market

Portability & Inter-operability → Reduced Life Cycle Cost
Evaluation

• Independent evaluation done (Summer 2007)

• Summary of Results (based on 8-slot chassis)
  ▪ 166 GFLOPS sustained throughput
  ▪ 4.6 FLOPS/byte (2G DDR2 per BCM1480 SoC)
  ▪ 136 MFLOPS/W computation efficiency
  ▪ 4.9 GFLOPS/Liter computation density (not counting I/O)

• Contact DRS for more details
For more information:

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Phone: 603-424-3750 x326
Octopus_support@drs-ss.com
http://www.drs-ss.com/capabilities/ss/processors.php
Backup Slides
VITA 41 (OCTOPUS) System Overview

- High Performance Embedded Multi-computing system backwards compatible with VME
- High Speed scalable advanced switch fabric with telecoms grade reliability
- Separate and redundant out-of-band (VITA 41.6) GigE control plane to every processing element
- Linux OS (SMP or ccNUMA)

- Octopus boards
  - Shown in standard VITA 41 chassis’
  - Sourced from commodity chassis vendor
  - Alternative backplane configurations exist and are supported as defined in VITA 41
• “Smart Switch” acts as Host controller
  ▪ Controls boot sequence
  ▪ Provides services to system

• Data Plane Connectivity
  ▪ Measured net 1.1 GBytes/s full duplex between any payload boards after fabric overhead and encoding/decoding
  ▪ Provides dynamic connectivity (no more static route tables) and single layer of switching between payloads

• Control Plane GigE Connectivity
  ▪ 1 GigE to every payload board and front panel
  ▪ 10 GigE between switch cards

• Dual Core Processor on board
  ▪ Each core running Linux at 600 MHz
  ▪ 256 MB DDR SDRAM at 125 MHz DDR memory bandwidth
  ▪ User (64 MB) and boot (4 MB) flash

• Temperature Sensors
  ▪ 1250 processor and each fabric switch
OCTOPUS Motherboard

• High performance **Quad Core** processor
  - MIPS64 SoC (System on a Chip) processor
  - 8 GFLOPS/processor (**32 GFLOPS/Chip**) with **4.8 GByte/s** composite I/O
  - Running SMP Linux at 1GHz on each core (ccNUMA capable)

• **2 GB** of **DDR2 SDRAM**
  - @200MHz

• **Flash**
  - User (128MB) and boot (4MB)

• **Front panel GigE and USB**

• **Power ~ 45W (Max)**

• **Temperature Sensors**
  - 1480 processor and fabric end-point
OCTOPUS Dual XMC

- VITA 42.4 compliant
- 2 x High performance Quad Core processors
  - MIPS64 SoC processors
  - Running SMP Linux at 1GHz on each core (ccNUMA capable)
- With each Quad Core processor:
  - **2 GB** of DDR2 SDRAM (3.2 GB/s)
  - 4 MB of flash
- Total of **8 x 1 GHz cores, 4 GB DDR2 SDRAM** and **8 MB boot flash**!
- Power ~ 65 W
- Temperature Sensors
  - For each 1480 processor
Fully loaded payload slot (Motherboard plus Dual XMC) provides:

- **96 GFLOPS** = 3 x High performance MIPS64 Quad BCM1480
- **6 GB** of DDR2 SDRAM
- Flash
  - User 128 MB
  - Boot 12 MB
- Node aliasing and ccNUMA
- On board PCI-X and HyperTransport
- Off board VITA 41 serial fabric
- Power ~ 110W (Max)
Inter-SoC Connectivity

Logical connectivity between Octopus Motherboard and daughtercard (XMC) CPU

BCM1480 SoC

HT/SPi switch

DDR-2 Memory

VITA 42.4 based XMC Connector

PCi-X I/O (PMC)

VME I/O

GigE I/O

Switch Fabric I/O

Maximum I/O bandwidth between SoC with HyperTransport running at 600MHz, 16-bit wide
Figures of Merit Comparison

- **Computation Efficiency (GFLOPS/Watt)**
- **Computation Density (GFLOPS/Liter)**

**Chassis with Radstone/PowerPC (G4DSP) card (not counting I/O bottlenecks)**

**DRS Octopus Chassis (counting I/O bottlenecks)**

**Note:** external I/O as needed via PMC sites in both systems

Advanced Processing Group
## Octopus SAR Benchmark Comparison

**Data Presented at Processor Technology Symposium on 10/3/06**

### Timing Results Normalized by Volume

Cell Processor software effort in process

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**Multi-core Board** | **Volume per Board** | **Gcc/Linux Multi-threading** | **Gcc/Linux Multi-threading Per cu. In.** | **Gcc/Linux Multi-processes** | **Gcc/Linux Multi-processes Per cu. In.** | **Vendor Compiler Multi-threading** | **Vendor Compiler Multi-processes** | **Vendor Multi-processes Per cu. In.**
--- | --- | --- | --- | --- | --- | --- | --- | ---
**Cu. Inches** | **Per cu. In.**
--- | --- | --- | --- | --- | --- | --- | --- | ---
Intel Sossaman | 756 | 26.2 | 2,817,157 | 19.45 | 3,794,834 | 28 | 2,636,054 | 19.8 | 3,727,754
Intel Dempsey | 756 | 23.2 | 3,181,445 | 12.2 | 6,049,961 | 20.5 | 3,600,465 | 9.93 | 7,432,983
Intel Woodcrest | 756 | 12.4 | 5,952,381 | 8.5 | 8,683,473 | 12.1 | 6,099,961 | 6.45 | 11,443,337
Intel Montecito | 3671 | 26.8 | 567,172 | 10.75 | 1,413,974 | 17.9 | 849,174 | 6.7 | 2,268,689
DRS-IT MIPS64 | 186.6 | 28 | 11,196,601 | 13.44 | 22,249,655 |  |  |  | 
Fabric7 Opteron | 2766 | 16.3 | 1,237,640 | 5.75 | 3,508,441 |  |  |  | 

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**Best SWaP Performance**
**Octopus Shows SWaP Advantage over Blade Servers**

**Recognizer Channel Performance for various processors**

- Intel Pentium 4 single core, hyperthread, 3.2 GHz (Pentium D 480), 130 W each
- DRS Octopus w/3 Broadcom chips, 900 MHz MIPS64/quad core, 20 W each
- Intel Pentium Dual Xeon 3.02 GHz, 130 W each
- IBM Cell processor, 60 W each
- Motorola Quad PowerPC VME 1.4 GHz, 20 W each
Development Environment
Advanced Debug Tools