Announcing PWRficient Processors from PA Semi, the Most Power Efficient, High Performance Processors Available

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September 20, 2007

PWRficient™
Cool, High-Performance MICROPROCESSORS

www.pasemi.com
The Escalating Power Problem

Shrinking device geometries provides:
- Faster gates
- Increased density

BUT

Moore’s Law means more power

EXCESSIVE POWER DISSIPATION LIMITS USABLE GATE CAPACITY
Choosing Power Over Ultimate Performance

- Look for the exponential opportunities in power/performance
- Give up some performance for substantial power decrease
Design Choices for Low Power

- Design choices at several levels favor low power
  - CMOS process target
  - Circuit design style and sizing
  - Micro-architecture features

- Integration
  - Saves interface power

- Management
  - Voltage/frequency scaling
  - Multiple power planes for optimal voltage selection per region
  - Clock gating to reduce power of idle circuits
  - Active and pre-charge standby modes in DRAM array
  - PCIe power saving modes
  - Nap and Sleep modes for CPU
Fine-Grained Clock Gating Reduces Dynamic Power

Coarse-Grained Clock Gating

Normal Operation

Worst Case

% of Flops Clocked

Time
Voltage/Frequency Scaling

- Multiple power planes for maximum control
  - VID regulators for cores, SoC
- Ability to scale both Vdd and frequency on demand results in highly optimized total power

<table>
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<th></th>
<th>Max Freq</th>
<th>Typ</th>
<th>Max</th>
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<tr>
<td>PA6T-1682M-FCN</td>
<td>2.0GHz</td>
<td>17W</td>
<td>25W</td>
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<tr>
<td>PA6T-1682M-FCG</td>
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<td>15W</td>
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<td>6W</td>
<td>10W</td>
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<tr>
<td>I/O coherent nap</td>
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<td>2W*</td>
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*PA6T-1682M-FCN nap power may be higher
Summary – The Green Computing Advantage

► PWRficient processors set the bar for ultimate energy conservation at full performance
  ▶ Lowest total energy for a computation or transaction

► PWRficient processors are designed to reduce system power
  ▶ Optional use of power standby mode in DDR2 memories

► Only minimal performance compromises to meet power-efficiency goals

► Significant operating-cost savings for cluster-based computing

► Power conservation a key initiative from architectural concept through design