

A Prototype FPGA Tile for Subthreshold-Optimized CMOS

Peter Grossmann (grossmann.p@husky.neu.edu), Miriam Leeser (mel@coe.neu.edu)
Northeastern University

Field-programmable gate arrays (FPGAs) are frequently used in low power systems because they can implement the same function as a microprocessor in a more energy-efficient manner while still offering the benefits of low development time and cost relative to an ASIC. The same could be true in ultra-low power applications operating at subthreshold supply voltages, where performance is sacrificed in favor of increased energy efficiency. Process technology research has demonstrated the benefits of tailoring device design to subthreshold operation. Subthreshold FPGA research is only beginning, and has yet to consider use of subthreshold-optimized devices. Simulation of an FPGA tile with a two-input logic block in a subthreshold-optimized FDSOI process is shown to demonstrate the potential benefits of this technology for subthreshold FPGAs, and to provide a starting point for a more thorough investigation into the best circuit design choices for subthreshold FPGA building blocks.

Motivation for Subthreshold FPGAs

Ultra-low power systems typically require some combination of custom integrated analog circuits (which may be analog, digital, or mixed signal) and/or ultra-low power microprocessor to meet system requirements and power goals. This has led some researchers to use subthreshold logic both for custom ASICs and microprocessors. Subthreshold circuits attain peak energy efficiency by using a supply voltage that is less than the threshold voltage of the transistors. The power savings obtained from this mode is significant since chip power scales with the square of the supply voltage. The tradeoff for running at such low voltages is an orders-of-magnitude sacrifice in performance. Presently, subthreshold logic is a reasonable design choice when operating frequencies in the tens or hundreds of kilohertz are acceptable. For some applications—such as wireless sensor nodes, digital hearing aids, and RFID tags—this can be the case.

Ultra low power systems turning to subthreshold logic would benefit from having a subthreshold FPGA option to implement digital components. A subthreshold FPGA offers several potential benefits, depending upon system requirements. In processor-based systems, a subthreshold FPGA can offer an energy-efficiency benefit. In ASIC-based systems, it can offer reconfigurability. In systems using both, it can enable the integration of the processor function and the ASIC function onto a single chip.

A subthreshold FPGA design has been presented for 90nm bulk CMOS[1]. Simulation of this design showed the energy-delay space accessible by the design for a representative logic function. Other simulations showed the challenges faced in implementing subthreshold FPGA routing circuitry due to process variation and a buffering scheme for mitigating that variation. The potential

performance gains from use of subthreshold-optimized devices were not explored in this work.

Benefits of Subthreshold-Optimized Device Technology

Research has shown that altering device design can improve performance for subthreshold operation. For bulk silicon, halo and retrograde doping are required for standard deep submicron transistors to suppress undesired short-channel effects. It has been argued that this is unnecessary for subthreshold because short-channel effects are reduced at ultra-low supply voltages. Eliminating these dopants reduces junction capacitance, which in turn improves delay and power consumption[2].

For fully-depleted silicon-on-insulator (FDSOI) transistors, another optimization can be made. Lightly doped transistors are desirable to reduce variation in threshold voltage both due to variation in oxide thickness and due to random dopant fluctuations[3]. In addition to performance benefits, subthreshold device optimizations for FDSOI thus have the potential to curtail the large performance variation seen in many subthreshold circuits to date. This technology is not yet mature, but the inherent advantages it holds over commercial bulk processes have been demonstrated at the device level. One goal of this work is to extend that demonstration to the circuit level through the development of subthreshold FPGA circuits.

Proposed Test Circuits

Figure 1 shows a template for an FPGA configurable logic block that will be used to investigate circuit tradeoffs for FPGA building blocks in subthreshold-optimized CMOS. The circuit consists of a two-input lookup table (LUT) with the LUT output connected to a D flip-flop. The output of the LUT and the output of the flip-flop are multiplexed so that either can be programmed as the CLB output. The LUT is SRAM-based with memory storage nodes tied to multiplexer inputs. The multiplexers perform table lookup based on logic inputs A and B. Input B is connected to the second-stage multiplexer and therefore has faster switching characteristics.

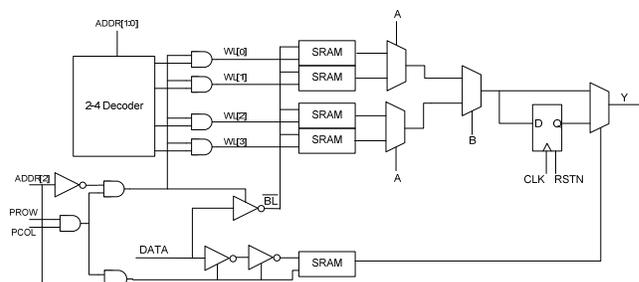


Figure 1: Configurable Logic Block (CLB) template.

