
**Abstract**

A Block Diagram Compiler (BDC) has been designed and implemented for converting graphic block diagram descriptions of signal processing tasks into source code to be executed on a Multiple Instruction Stream - Multiple Data Stream (MIMD) array computer. The compiler takes as input a block diagram of a real-time DSP application, entered on a graphics CAE workstation, and translates it into efficient real-time assembly language code for the target multiprocessor array. The current implementation produces code for a rectangular grid of Texas Instruments TMS32010 signal processors built at Lincoln Laboratory, but the concept could be extended to other processors or other geometries in the same way that a good assembly language programmer would write it. This report begins by examining the current implementation of the BDC including relevant task-assigment aspects of the target hardware. Next, we describe the task-assigment module, which uses a simulated annealing algorithm to assign the processing tasks of the DSP application to individual processors in the array. Finally, our experiences with the current version of the BDC software and hardware are reported.