Monday, September 26, 2011
7:30 a.m. REGISTRATION OPENS – UNTIL 5:00 PM
7:30 – 8:30 a.m. BREAKFAST
8:30 – 8:55 a.m. OPENING REMARKS
Steven Vitale, MIT Lincoln Laboratory, Conference Chairman

SESSION 1 SUBTHRESHOLD DEVICES AND TECHNOLOGY
8:55 – 9:00 a.m. Introduction: Chenson Chen, MIT Lincoln Laboratory, Chair
9:00 – 9:40 a.m. Invited: Energy Efficient Designs with Wide Dynamic Range
Vivek De, Intel
9:40 – 10:00 a.m. Design of SOTB MOSFET for Super Low Voltage, Low-Power Applications
T. Iwamatsu, Low-Power Electronics Assoc & Project (LEAP)& Renesas, Japan
10:00 – 10:20 a.m. Ultra-Thin SOI substrates: performance improved options readiness
W. Schwarzenbach, Parc Technologique des Fontaines, Bernin, France
10:20 – 10:40 a.m. Break
10:40 – 11:00 a.m. Demonstration of 0.7-V Opamp for Scaled Technology
S. O’uchi, National Institute of Adv IndustrSci and Tech, Ibaraki, Japan
11:00 – 11:20 a.m. Ultra-low power subthreshold-triode operation for current mode circuits
K.P. Lam, The Chinese University of Hong Kong, Shatin, Hong Kong
11:20 – 11:40 a.m. On-chip Energy Harvesting and Active Cooling Using Silicon-based
Nanostructured Thermoelectrics
Z. Aksamija, University of Wisconsin-Madison
11:40 – 12:00 a.m. Characteristics of MOSFET devices in subthreshold region
N. Kamin, University of Hawaii at Manoe
12:00 – 1:00 p.m. LUNCH

SESSION 2 RF AND ANALOG CIRCUITS
1:00 – 1:05 p.m. Introduction: Chang-Lee Chen, MIT Lincoln Laboratory, Chair
1:05 – 1:45 p.m. Invited: A 2.4GHz, 0.65V Single Supply Wireless Sensor Node with 0.95nJ/b Link Energy
T. Fiez, Oregon State University
1:45 – 2:05 p.m. A 0.5V ultra low power sub-threshold FDSOI transconductance amplifier
K. Park, Tufts University
2:05 – 2:25 p.m. Sub-threshold RF Characteristics of Partially-Depleted SOI MOSFETs
M. Emam, ICTEAM Institute, Universite catholique de Louvain, Belgium
2:25 – 2:35 p.m. Break
2:35 – 2:55 p.m. RF-only Logic Circuits
P. Gatfort, North Carolina State University
2:55 – 3:15 p.m. Analog Signal Processing for Emerging Ultra Low Power Broadband Electronic Systems
J. Laskar, InSite Partners, Cupertino, CA
3:15 – 3:35 p.m. Break
SESSION 3  MEMORY AND DIGITAL CIRCUITS - PART I
3:35 – 3:40 p.m. Introduction: Jeff Knecht, MIT Lincoln Laboratory, Chair
3:40 – 4:20 p.m. 0.5-V High-Speed Circuit Designs for Memory-Rich Nanoscale CMOS LSIs
K. Itoh, Central Research Laboratory, Hitachi, Ltd., Japan
4:20 – 4:40 p.m. A 72Kb Single-Ended Disturb-Free Subthreshold SRAM with Cross-Point Data-Aware Write Word-Line, Negative Bit-Line, and Adaptive Read Operation Timing Tracing
M-H. Tu, National Chiao Tung University, Hsinchu, Taiwan
4:40 – 5:00 p.m. Stability oriented SRAM performance optimization in subthreshold operation
A. Makosiev, Institut Superieur d'Electronique de Paris, France
5:00 – 5:20 p.m. Analyzing Subthreshold Bitcell Topologies and the Effects of Assist Methods on SRAM min
J. Boley, University of Virginia
5:20 – 6:30 p.m. Posters and Reception
To be updated 08-15-11
6:30 – 8:30 p.m. Banquet and Invited Speaker

Tuesday, September 27, 2011

7:30 a.m. REGISTRATION OPENS
7:30 – 8:00 a.m. BREAKFAST
SESSION 4  BIOMEDICAL APPLICATIONS AND RADIATION EFFECTS
8:00 – 8:05 a.m. Introduction: Pascale Gouker, MIT Lincoln Laboratory, Chair
8:05 – 8:45 a.m. Ultra Low Power Bioelectronics
R. Sarpeshkar, MIT
8:45 – 9:05 a.m. Sub-threshold Computational Circuits for High-order Data-driven Analysis of Physiological Signals
S. Mohammed, Princeton University
9:05 – 9:25 a.m. Subthreshold VLSI design of a phase-locked loop inspired by a biological neural integrator
Y. Meng, MIT
9:25 – 9:35 a.m. Break
9:35 – 9:55 a.m. Ultra Low Power, LPF-Only DWT Architecture for an Epileptic Seizure Prosthesis Implant
M. Sharad, Purdue University
9:55 – 10:15 a.m. A Low-power Single-Bit Continuous-time ΔΣ Converter with 92.5dB Dynamic Range for Biomedical Applications, and design of Ultra-low Voltage ΔΣ ADCs
S. Balagopal, Boise State University
10:15 – 10:35 a.m. Subthreshold microelectronic design of a wide-dynamic-range silicon synapse
Y. Meng, MIT
10:35 – 10:55 a.m. Heavy Ion Characterization of a Novel Radiation Hardened Flip-Flop at Sub- and Super-Threshold Voltage Operation
A. Chavan, University of Texas
10:55 – 11:15 a.m. Break
SESSION 5  MEMORY AND DIGITAL CIRCUITS - PART II
11:15 – 11:20 a.m.  Introduction: Jeff Knecht, MIT Lincoln Laboratory, Chair
11:20 – 11:40 a.m.  Circuit-Level Considerations for an Ultra-Low Voltage FPGA with Unidirectional, Single-Driver Routing Fabric
                       P. Grossman, Northeastern University
11:40 – 12:00 p.m.  Mitigating Variation in Subthreshold FPGAs with Component-Specific Routing
                       N. Mehta, California Institute of Technology
12:00 – 1:00 p.m.   LUNCH
1:00 – 1:20 p.m.   A sub-threshold clock and data recovery circuit for a wireless sensor node receiver
                       A. Shrivastava, University of Virginia
1:20 – 1:40 p.m.   Design Methodology for Sizing DC-DC Converters Supplying Subthreshold Circuits
                       J. De Vos, ICTEAM Institute, Universite catholique de Louvain, Belgium
1:40 – 2:00 p.m.   A Programmable Multi-channel Sub-threshold FIR Filter for a Body Area Sensor Node
                       A. Klinefelter, University of Virginia
2:00 – 2:20 p.m.   300 mv Operated Asynchronous Pipelined ALU with Straintronics-based nonvolatile latch for Ultra-Low Power Applications
                       H. Liu, University of Michigan
2:20 – 2:40 p.m.   Optimal Power Switch Design for Panoptic Dynamic Voltage Scaling enabling Sub-threshold Operation
                       K. Craig, University of Virginia
2:40 – 3:00 p.m.   Break
3:00 – 3:20 p.m.   Exploring the Opportunity of Operating a COTS FPGA at 0.5V
                       F. Botman, ICTEAM Institute, Universite catholique de Louvain, Belgium
3:20 – 3:40 p.m.   Exploration Analysis of Process Variation Sensitivity in Risc-like Microprocessors Operating at Low Supply Voltages
                       S. Moreno Londono, Eindhoven University of Technology, Eindhoven, the Netherlands
3:40 – 4:00 p.m.   Preliminary Measurements of a Subthreshold Timing Error Detection Microcontroller
                       L. Koskiken, Aalto University, Finland
4:00 – 4:20 p.m.   Designing, Fabricating, and Testing Noise Immune Circuits
                       M. Donato, Brown University
4:20 – 4:40 p.m.   Subthreshold Design of Physical Unclonable Functions
                       S. K. Srivaths, University of Massachusetts, Amherst
4:40 – 5:00 p.m.   Wrap-up – Conference Chair