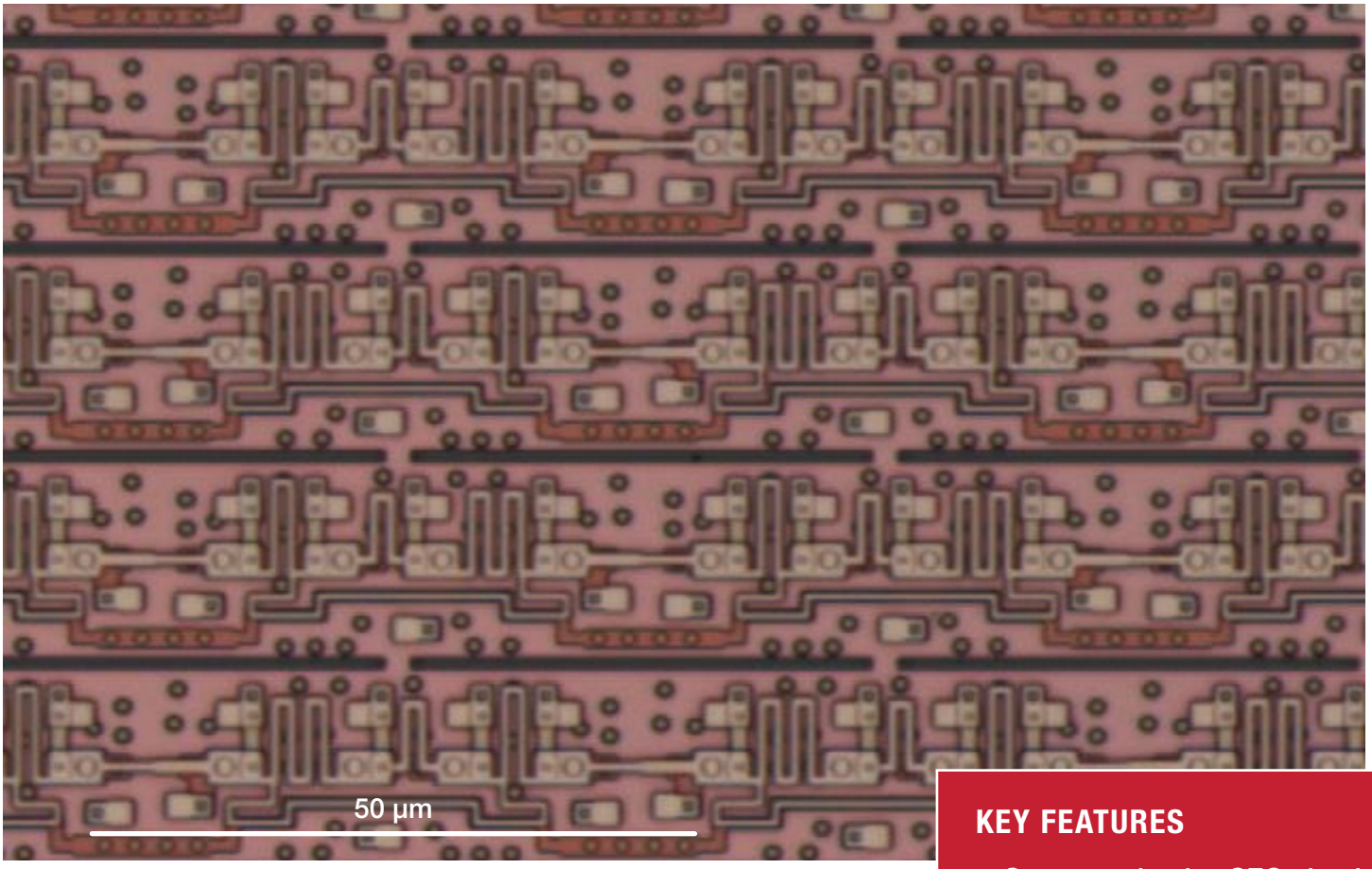
MICROELECTRONICS LABORATORY

SPOTLIGHT ON

Superconducting Integrated Circuits



Photomicrograph of superconducting single-flux-quantum (SFQ) shift-register integrated circuit fabricated at Lincoln Laboratory.

MIT Lincoln Laboratory has developed the world's most advanced single-flux-quantum (SFQ) integrated circuit process. This research foundry capability enables prototyping of advanced SFQ circuits along with flip-chip packaging on superconducting multi-chip modules.

KEY FEATURES

- Superconductive SFQ circuits with fast switching speed and low switching energy unmatched by any other demonstrated integrated circuit technology
- SFQ circuits demonstrated with up to 809,000 Josephson junctions, a world record
- Cryogenic operation

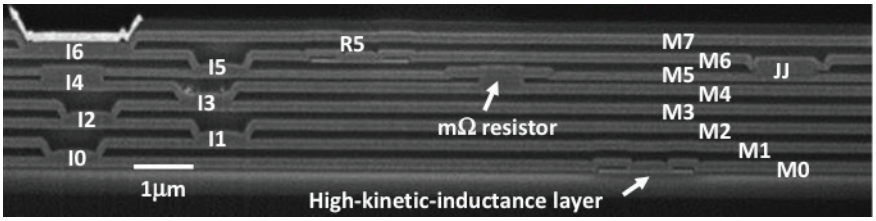
Lincoln Laboratory Processes

Multiple SFQ research foundry fabrication process nodes are either offered or under development as outlined in the MIT Lincoln Laboratory SFQ Technology Roadmap. The table below outlines key features and dimensions offered for each process node. By adding more wiring layers, incorporating stud vias, and reducing minimum linewidths, higher circuit densities can be achieved. New process features are first made available to circuit design teams while the process is matured. A new high-J_C process, SFQ5hs, is available for 2017. Future nodes, such as SFQ7ee, will feature additional wiring layers and reduced minimum feature sizes.

Fabrication Process Attribute		Units	Process Node					
			SFQ3ee	SFQ4ee	SFQ5ee	SFQ6ee	SFQ5hs	SFQ7ee
Critical current density		MA/m^2	100	100	100	100	200	100
JJ diameter (surround)		nm	700 (500)	700 (500)	700 (500)	700 (300)	700 (500)	500 (200)
Nb metal layers		–	4	8	8	9	8	10
Line width (space)	Critical layers	nm	500 (1000)	500 (700)	350 (500)	350 (400)	350 (500)	250 (300)
	Other layers	nm			500 (700)	500 (700)	500 (700)	350 (500)
Metal thickness		nm	200	200	200	200	200	200
Dielectric thickness		nm	200	200	200	200	200	200
Resistor width (space)		nm	1000 (2000)	500 (700)	500 (700)	500 (700)	500 (700)	500 (500)
Shunt resistor value		Ω/sq	2	2	2 or 6	2 or 6	2 or 6	2 or 6
mΩ resistor		mΩ	–	–	3–10	3–10	3–10	3–10
High kinetic inductance layer		pH/sq	–	–	8	8	8	8
Via diameter (surround)		nm	700 (500)	700 (500)	500 (500)	500 (500)	500 (500)	350 (250)
Via type, stacking		–	Etched, staggered	Etched, stacked \2/	Etched, stacked \2/	Stud, stacked \2/	Etched, stacked \2/	Stud, stacked
Early access availability		–		2014	2015	2016	2017	2018

Red text indicates changes from the previous process.

SFQ5ee Process Node



Cross section of an SFQ integrated circuit fabricated in Lincoln Laboratory's SFQ5ee process node. The eight Nb wiring layers (M0–M7) are visible along with etched vias (I0–I6). The Josephson junction (JJ) is placed between M5 and M6. The resistor layer (R5), the milliohm (mΩ) resistor, and the high-kinetic-inductance layer are also indicated.

The SFQ5ee process provides attractive features:

- 700-nm Josephson junctions
- Eight Nb wiring layers
- 350-nm wiring feature size
- High-kinetic-inductance layer

Applications

Our SFQ integrated circuits can have application in a variety of fields:

- High-performance digital computing
- Wideband mixed RF/digital processing
- Quantum computing

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