Digital-Pixel Focal Plane Array Technology

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Lincoln Laboratory has developed a digital-pixel focal plane array with per-pixel, 16-bit full dynamic range, analog-to-digital conversion, and real-time digital image processing capability. The technology leverages modern semiconductor processes to achieve low-power, high-component-density designs. Infrared sensors based on this innovative technology are enabling very-wide-area, high-resolution, high-sensitivity, high-update-rate imaging, as well as novel sensing modalities.

» **Many emerging thermal infrared (IR)** sensing applications simultaneously demand high sensitivity, large dynamic range, large pixel count, and operation at fast data rates. Among these applications are day/night persistent surveillance, border patrol and protection, aerial search and rescue, and environmental remote sensing. Such applications typically require sensor systems capable of high-quality, large-pixel-count images; furthermore, in many cases, the images must be processed rapidly to extract time-critical information. For example, real-time feature extraction that localizes a region of interest can be a key component of a high-resolution, wide-area imaging system. These requirements are driving the demand for high-capacity image processing.

Another much-sought-after demand is the ability to integrate real-time, high pixel-count, image-based sensor systems into low size, weight, and power (SWaP) packages to enable the integration of the systems into a wide range of platforms. However, the development of such low-SWaP, high-performance sensor systems poses significant challenges for conventional focal plane array (FPA) technologies, which have limited data rate, dynamic range, and on-chip processing capabilities. While conventional technologies perform well in limited circumstances, scaling the technologies to meet these emerging demands is difficult and results in large, complex, expensive systems. The digital-pixel focal plane array (DFPA) was developed to address the shortfalls of conventional FPAs.

The DFPA combines a commercially produced detector array with a digital-pixel readout integrated circuit (DROIC) designed by Lincoln Laboratory; this compat-

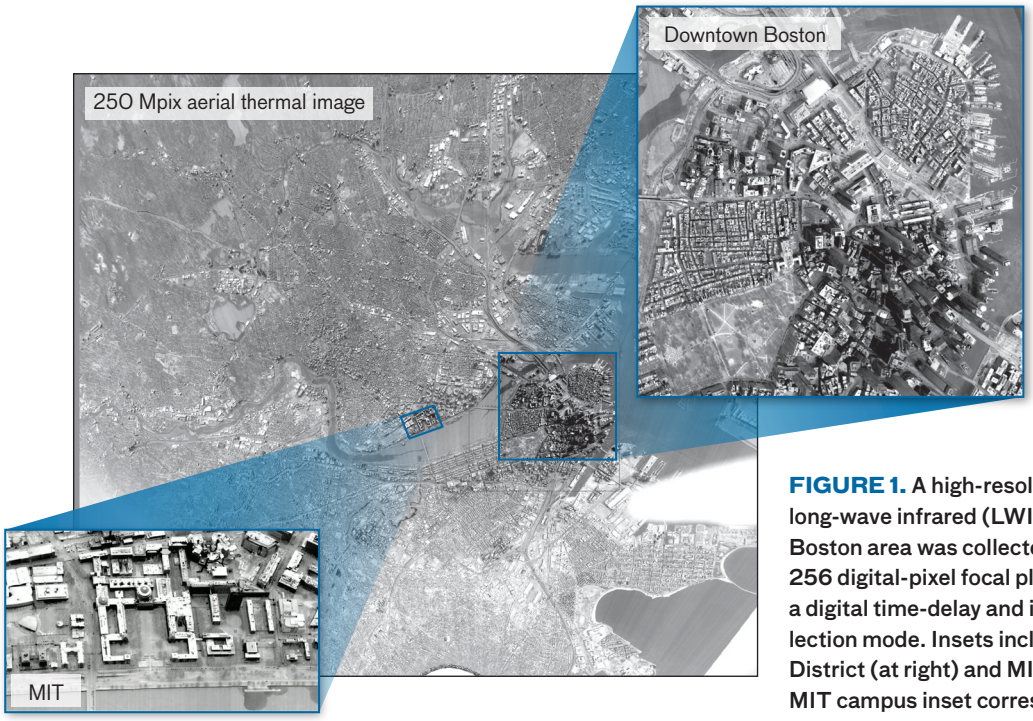

FIGURE 1. A high-resolution, 250-megapixel, long-wave infrared (LWIR) image of the greater Boston area was collected at night using a 256 × 256 digital-pixel focal plane array operating using a digital time-delay and integrate (TDI) data collection mode. Insets include the Boston Financial District (at right) and MIT campus (lower left). The MIT campus inset corresponds to approximately a 1-megapixel image, representative of state-of-the-art large format LWIR focal plane array technology.

ibility between available detector technology and the specialized DROIC allows the DFPA technology to be adapted to existing systems. The DROIC includes a low-power analog-to-digital converter in every pixel [1]. The primarily digital nature of a DFPA pixel, as opposed to the primarily analog pixel employed in other analog- and digital-output ROIC devices, offers the potential for a rapid development process that exploits digital component libraries.

The DFPA's innovations enable design flexibility and the possibility to revolutionize thermal imaging systems. The DROIC has been demonstrated with a variety of different detector wavebands—for instance, short-wavelength and long-wavelength infrared—and detector technologies, such as conventional p-n junction photodiodes and band-gap engineered materials. Prototype sensor systems employing DFPA technology have been developed and field-tested. The imagery in Figure 1 highlights DFPA-enabled capabilities.

Conventional Focal Plane Array Technology

As with modern digital photography and video recording cameras, the heart of a long-wavelength infrared (LWIR) thermal imaging sensor is the focal plane array—the device that converts an optical image into an electrical signal that can then be read out and processed and/or stored. While visible-light-sensitive FPAs can be fabricated with the same silicon-based integrated circuit (IC) materials and techniques used to produce processors and memory, these materials are not sensitive to LWIR radiation. Thus, LWIR detectors must be fabricated by using alternative materials and less-well-developed fabrication processes. The resulting devices have smaller pixel counts, lower yields, and higher pixel-to-pixel variability. In the fabrication of a working LWIR FPA, the detector array must be mated to a readout integrated circuit whose basic function is to accumulate and store the detector photocurrent from each pixel and to transfer the resultant signal onto output ports for readout (Figure 2). To achieve maximum sensitivity, the LWIR FPA is integrated into an evacuated dewar and cryogenically cooled to minimize thermally generated current.

In conventional analog ROIC technology, the photocurrent generated by a detector is accumulated and stored locally in a capacitor (electron well); the maximum charge stored during an integration time is equal to the product of the total capacitance and the maximum

allowable voltage across the capacitor. A simplified ROIC unit cell (pixel) circuit diagram and example ROIC layout are presented in Figure 3. The circuit consists of a low-noise input amplifier—primarily used to isolate the detector bias from the following unit cell circuits—that feeds an integrating capacitor. Simple switching and buffer circuits are used to connect the integrating capacitor voltage (proportional to the stored photoelectrons) to a multiplexor circuit for readout. As indicated in Figure 3, the integrating capacitor dominates the unit-cell area usage. Given technology limitations (i.e., process-limited voltage and capacitance density), local storage is typically limited to <25 million photoelectrons in a 30 □m pitch pixel; a 25-million-photoelectron well can be obtained with a maximum 5 volts across a 0.8-picofarad integrating capacitor. After an image is collected, the resultant charge-based image representation is transferred to a set of output ports for subsequent analog-to-digital conversion and processing on a row-by-row or columnar basis. This transference is typically accomplished by using a multiplexor architecture in which the voltage at each pixel (equal to the stored photodetected charge divided by the electron well capacitance) is sequentially transferred onto an analog bus and routed onto the output ports.

The unit-cell well depth fundamentally determines the maximum sensitivity of an FPA; assuming a well-designed ROIC in which the total noise is set by the inherent statistical fluctuations of the signal-derived photocurrent (i.e., shot-noise limited detection), the maximum signal-to-noise ratio (SNR) is achieved when

$$SNR_{Max} = \frac{Signal_{Max}}{Noise} = \frac{N_{Well}}{\sqrt{N_{Well}}} = \sqrt{N_{Well}}$$

where $Signal_{Max}$ represents the maximum measurable signal in units of photoelectrons (detected charge) and *Noise* represents the Poisson-process-limited statistical variation associated with the detected photoelectron signal. A maximum well depth equal to 25 million photoelectrons results in a maximum shot-noise-limited SNR of 5000 (12.3 bits).[1]

With the detected photocurrent now stored at each unit cell, the ROIC must read out the analog charge for subsequent use. The technical challenge is to maintain the SNR (dynamic range) while minimizing the number of output ports (and corresponding dewar penetrations). Current analog-to-digital converters (ADC) support 14-bit dynamic range at a data rate of 20 megapixels per second [3]. Thus a 1-megapixel image can be read out at a 30 Hz video frame rate with 14-bit dynamic range with two high-speed output ports.

The maximum well limitation, together with the limitation on the maximum allowable data rate per output port, poses technical challenges to developing large-format FPAs that operate at or near maximum sensitivity. Consider the example scenario of an f/2 camera observing a mean background scene temperature of 300 K. In this example, a 25-million-photoelectron well fills in approximately 0.3 ms, requiring an image data rate of 3300 frames per second to maintain near-constant signal integration (i.e., to achieve maximum sensitivity). A 1-megapixel image reading out at 3.3 kHz would require 165 output ports operating at 20 megapixels per second per port! While many applications do not require continuous signal integration (for maximum sensitivity), it will be challenging to scale conventional analog ROIC technology to emerging, high-sensitivity, high-pixel-count applications.

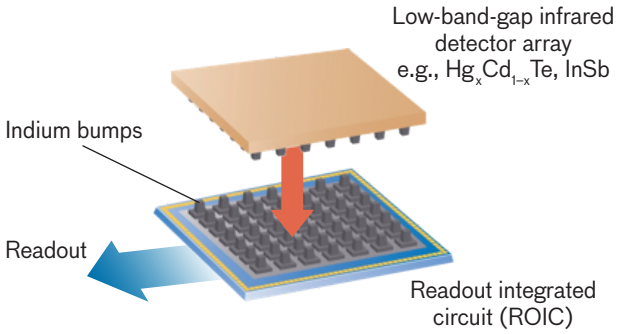

FIGURE 2. Components of an infrared (IR) focal plane array. Detector photodiodes fabricated using low-band-gap materials (e.g., mercury cadmium telluride [HgCdTe] or indium antimonide [InSb]) are bonded to a silicon complementary metal-oxide semiconductor (CMOS) readout integrated circuit (ROIC); soft metal indium bumps are used to facilitate the detector/ROIC hybridization process. The IR detectors generate photocurrent proportional to the incident IR radiation; the ROIC stores the photocurrent at each pixel site and routes the signal onto a limited set of output ports for later exploitation.

1. SNR is defined for spatially resolved objects.

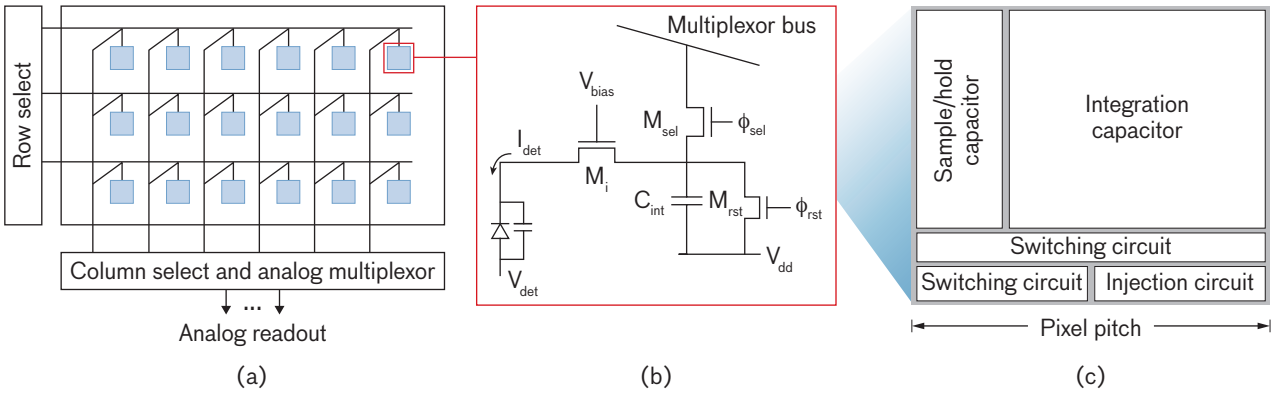

FIGURE 3. (a) Analog ROIC architecture with (b) simplified unit-cell or pixel circuit diagram and (c) unit-cell layout. As shown in (b), photocurrent I_{det} is generated by the photodiode and subsequently integrated onto the capacitance C_{int} through the injection transistor M^i, which also provides the photodiode bias V_{bias}. The signal voltage across C_{int} can be switched onto the multiplexor bus for readout via control signal ϕ_{sel} on switch M_{sel} [2]; the signal voltage across C_{int} can be reset by control signal ϕ_{rst} using switch M_{rst}. A maximum 2.2-volt process (set by V_{dd}) and C_{int} equal to 1850 femtofarads results in a maximum stored photocharge equal to 25 million electrons. Note that circuit capacitance as shown in (c) dominates the pixel footprint.

Digital-Pixel Readout Integrated Circuit Technology

The DFPA technology developed at Lincoln Laboratory exploits the unique DROIC and overcomes the limitations of conventional analog FPAs by performing in-pixel signal digitization. The DFPA enables a larger dynamic range, a faster low-noise all-digital readout, and on-chip processing for reduced sensor SWaP and for the development of novel sensing modalities [4–7]. The technical approach enables sub-20 □m pitch, low-power designs by employing simple, compact circuits, such as low-power analog-to-digital conversion circuits, as well as low-power counters and shift registers.

Structure of the Basic DROIC Unit Cell

The basic DROIC unit-cell circuit and example unit-cell layout are presented in Figure 4. The components include a preamplifier/buffer, an in-pixel analog-to-digital converter consisting of a photocurrent-to-frequency converter (I-to-F converter) circuit connected to a counter/shift register, multiplexors to connect the counter/shift register to one of four nearest-neighbor unit cells, and pixel timing and control circuits.

The digital unit cell is configurable. The conversion gain (equivalent to the least significant bit [LSB] of the digitization process) of the I-to-F converter can be adjusted (i.e., the frequency for a given input current can be adjusted) to maximize the electronic well depth (maximum value of LSB) or minimize quantization noise (minimum value of LSB); the counter/shift register can be preset to any value and can be configured to increment or decrement the register contents; the counter can be reconfigured as a shift register; and the multiplexor can be configured to connect the register contents into any one of four nearest-neighbor unit cells. The counter can be partitioned into two independently controlled counters, i.e., each counter can be independently controlled to increment or decrement the I-to-F output pulse train.

As in the case of an analog unit cell, a preamplifier (direct-injection transistor) is used to isolate the detector bias from the unit-cell circuits. The buffered photocurrent is then applied to a small (parasitic) integrating capacitance (C_{int}) of approximately 1 femtofarad, which corresponds to a maximum charge bucket of approximately 6000 photoelectrons assuming a maximum of 1 volt across C_{int}. Compare this to an analog unit cell's full well capacity of 25 million photoelectrons. As the charge bucket fills, the voltage V across C_{int} increases as $\Delta V = \Delta Q / C_{int}$, where ΔQ is the change in the current Q. When the voltage V reaches a preset threshold, a comparator circuit is tripped. The output of the comparator is fed to (1) a circuit that resets the voltage across the integrating capacitor and (2) a pulse-generation circuit that is input to an N-bit digital counter.

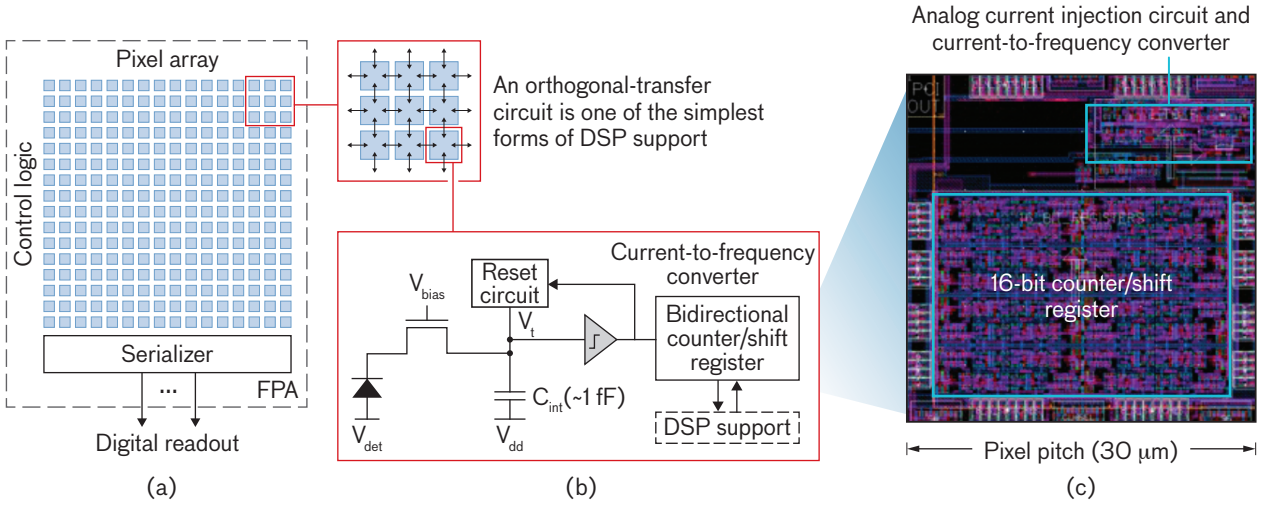

FIGURE 4. (a) Digital ROIC (DROIC) architecture with (b) simplified unit-cell circuit diagram and (c) unit-cell layout. As shown in (b), an injection transistor feeds a small integrating capacitor (~1 femtofarad) corresponding to an electron well of ~6000 electrons at a maximum of 1 volt across the integrating capacitor. When the well fills, the integrating capacitor charge is reset and a pulse is generated, resulting in a pulse train with frequency proportional to the input photocurrent, with each pulse incrementing or decrementing a counter depending on the initial configuration. Simple digital signal processing (DSP) operations can be applied during signal integration. When the shutter is closed, the counter represents the total number of times the electron well filled; with the well size known, the counter contains the digital representation of the number of integrated photoelectrons. The contents of the 16-bit counter/register can be shifted to any of its four nearest neighbors and read out by using high-speed digital readout circuits. Note that the 16-bit counter (c) dominates the pixel footprint.

Operation of the Digital Unit Cell

Prior to the opening of the electronic shutter, the unit cell is configured (e.g., the counter is preset to an initial value and programmed to increment its contents with each input pulse), and the integrating capacitor is reset. When the shutter opens, the small integrating capacitor fills at a rate proportional to the photocurrent (which itself is proportional to the in-band light incident on the detector), and the progression of charging and resetting generates a pulse train whose frequency is proportional to the photocurrent. The pulse train is input to the N-bit counter, which then increments (or decrements) its contents with each pulse until the shutter is closed, at which point the contents of the counter represent a "digital" well with total integrated photoelectrons equal to the product of the digital count and the (known) well capacity.[2] In this way, the photocharge on the integrating capacitor can be interpreted as the charge associated with a single digital count, i.e., the least significant bit of the digital counter. The quantization noise associated with the analog-to-digital conversion process is given by [8]

$$\text{Quantization Noise} = \sqrt{LSB/12} = \sqrt{Q/12}$$

where $Q = (V_t - V_{dd}) \times C_{int}$ is the effective well size (in electrons), C_{int} is the integrating capacitor, V_t is the comparator voltage threshold, and V_{dd} sets the initial voltage across the integrating capacitor. The digital signal can now be routed to one of four neighboring pixels (based on the initial unit-cell configuration) and noiselessly shifted at high speed. Serializer circuits located at the edge of the array stream data onto high-speed (nominal 2 Gbps) line drivers.

Digital Readout Integrated Circuit Design Parameters

Design parameters of representative DROIC devices are provided in Table 1. Devices have been fabricated using an IBM 90 nm and 65 nm low-power digital integrated circuit process that, to date, enables up to ~2000 transistors

2. The counter can be configured to increment or decrement pulses independent of the shutter time (i.e., total signal integration time); by alternating between increment and decrement modes, the DFPA can effectively AC couple the input signal.

to be integrated within a single digital unit cell as small as 12 □m. The digital pixel contains approximately 100 times the number of transistors contained in a typical analog unit cell. The deeply scaled 90 □m IC process enables dual-polarity input circuits [9], 16-bit register, orthogonal transfer, and control and signal circuits in a 30 □m pitch unit cell. Once digitized, the data can be streamed off chip on four 2 Gbps output ports; a 16-bit, 256 × 256 pixel image can be read out at a frame rate of 7 kHz.

Advantages of the Digital-Pixel Focal Plane Array

The elemental components of the basic digital unit cell—a digital counter/shift register configurable to increment or decrement at a rate proportional to the input photocurrent, a configurable multiplexor enabling an orthogonal-transfer data structure, and high-speed data input/output—together enable a low-power, high-dynamic-range imager that provides an on-chip image processing capability and that affords significant advantages over conventional analog unit-cell technology [5, 6].

Ultrasensitive Imaging

With a conversion gain (electrons per digital count) equal to 3500, the 16-bit digital well corresponds to ~230 million photoelectrons or approximately 10 times the analog well capacity of 25 million photoelectrons. Under ideal (shot-noise-limited) performance, the larger digital well would translate to a factor of 3 improvement in SNR; a factor of 2.5 improvement (limited by low-frequency noise) can be achieved, as shown in Figure 5. The DFPA can, however, be operated to further increase effective

Table 1. Digital-Pixel Readout Integration Circuit Parameters

DROIC FEATURES	CURRENT	FUTURE
Manufacturing process	65–90 nm	≤32 nm
Format	256 × 256 640 × 480	1280 × 720 4028 × 4028
Pitch	20 μm 30 μm	≤12 μm
Bits	14–21	>28
Digital count	~3000–6000 electrons	<100 electrons
Wavelength	SWIR–LWIR	Visible-VLWIR
Data rate	Up to 32 Gbps	100 Gbps
Orthogonal transfer	Yes	Yes
In-pixel computation	• Up-down counter – Background subtraction – Spatial filtering • Split counter – 2-kernel spatial filtering – In-phase and quadrature AC signal detection – Compressive sensing – Multifunction sensing	• Multiple independently controllable counters – Temporal matched filtering • Threshold detection logic

sensitivity by (1) suppressing low-frequency noise (and other slowly varying additive background components) by periodically subtracting out background variations and (2) exploiting the fact that the digital counter value is equal to Mod[Pulse Count, 2^{Bits}]. Unlike an analog pixel, which saturates at the maximum well capacity, the digital pixel "rolls over" when the pulse count exceeds 2^{Bits}, thus effectively increasing the bit depth.

Because LWIR detectors typically exhibit low-frequency noise, most high-performance LWIR imaging systems employ low-frequency noise-suppression techniques to achieve near shot-noise-limited sensitivity. These techniques, collectively referred to as nonuniformity compensation techniques, are based on estimating the slowly varying pixel response at a rate sufficient to capture the pixel-to-pixel, low-frequency, noise-induced, additive spatial variations (and slowly varying background components) and subtracting this estimate from subsequent imagery. Through the use of conventional analog detector arrays, a background image is collected (e.g., by observing a flat-field calibration plate) when needed and stored off chip. As imagery is collected, the background estimate is subtracted off chip. With the use of a DFPA, a background image can be collected with the counter in decrement mode (i.e., a "negative" background image is collected). With the digital counter now preset to the negative of the background, the counter is configured to increment pulses and the desired scene data are collected; in this way, the background is effectively subtracted from the image on chip.

Because the background typically represents a significant fraction of the total integrated in-pixel charge, the suppression of the background effectively increases the dynamic range (as the available bit depth need only span the signal minus the background). This process—collect background image in decrement mode, collect scene image in increment mode—can be repeated until the integrated signal achieves the maximum well depth. The nonuniformity compensation process can be implemented entirely on chip with a significant improvement

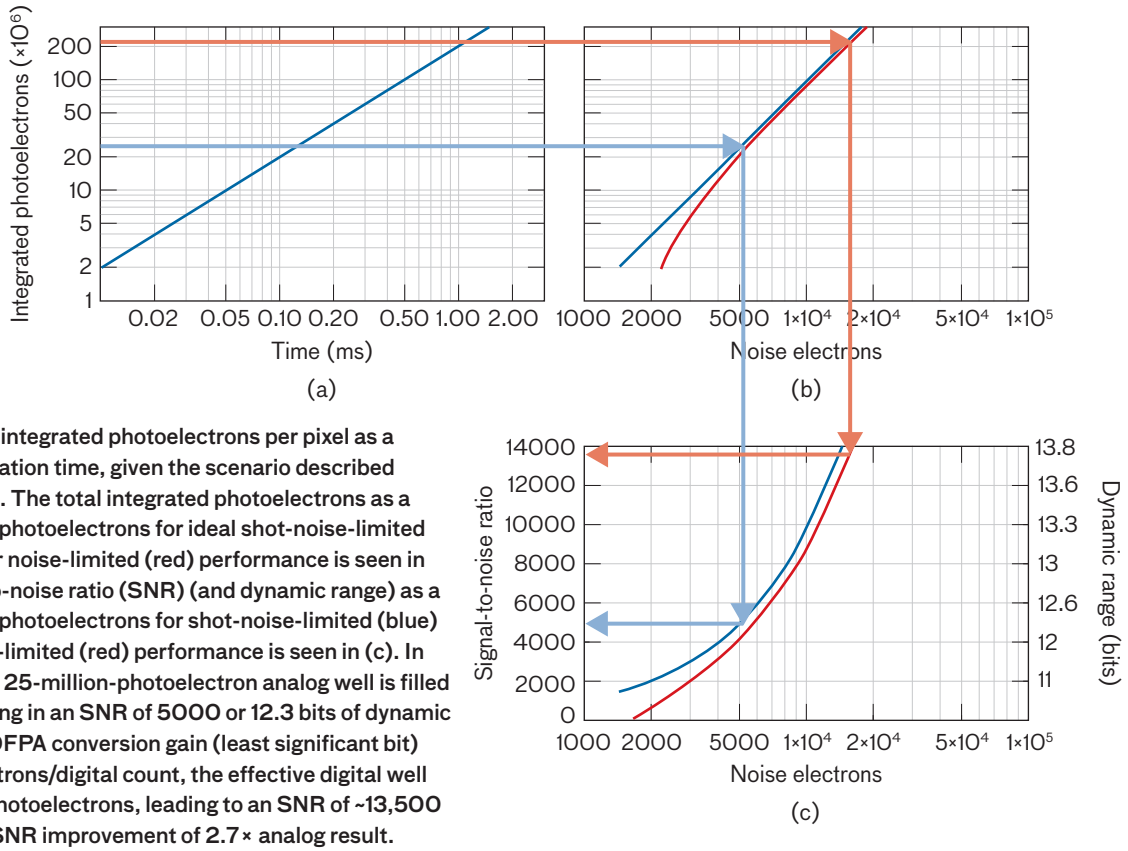

FIGURE 5. The integrated photoelectrons per pixel as a function of integration time, given the scenario described in Appendix A (a). The total integrated photoelectrons as a function of noise photoelectrons for ideal shot-noise-limited (blue) and sensor noise-limited (red) performance is seen in (b). The signal-to-noise ratio (SNR) (and dynamic range) as a function of noise photoelectrons for shot-noise-limited (blue) and sensor noise-limited (red) performance is seen in (c). In this example, the 25-million-photoelectron analog well is filled in 0.3 ms, resulting in an SNR of 5000 or 12.3 bits of dynamic range. With the DFPA conversion gain (least significant bit) set to 3500 electrons/digital count, the effective digital well is ~230 million photoelectrons, leading to an SNR of ~13,500 (~13.7 bits)—an SNR improvement of 2.7× analog result. Sensor parameters used in the calculations are provided in Appendix A. The noise model is provided in Appendix B.

in sensitivity by exploiting the increased digital well. In this example, only 50% of the available integration time is used to collect the image (the remaining 50% is used to estimate the time-varying background image). However, if the background drift rate is much slower than the total signal integration time, then the background could be collected less frequently and the total signal integration efficiency could be increased.

Electronic On-Chip Image Stabilization

High-speed orthogonal transfer (i.e., the ability to perform on-chip image translation) enables efficient signal integration in the presence of line-of-sight motion. Specifically, knowledge of the line-of-sight angle movement (e.g., using an inertial measurement unit) can be used to stabilize the image on chip for continuous signal integration without the need for high-speed readout. This capability is demonstrated in Figure 6, which shows a resolved image that has been stabilized.

(a) (b)

FIGURE 6. The DFPA enables image stabilization by using an inertial measurement unit to drive data transfer between pixels. In this example, a short-wave infrared DFPA imaged a clock with a 250 ms integration time; (a) was imaged without image stabilization and (b) with on-chip image stabilization.

Ultra-Large Pixel Count Infrared Imagery

Limitations of LWIR detector fabrication processes and the need for cryogenic operation to reduce detector dark current pose challenges to developing high-operability, ultra-large-pixel-count (e.g., 1000 megapixels) cameras. While scanning techniques have been used to obtain large-format imagery, frame-rate needs typically limit detector integration times and hence detection sensitivity. The ability of the DFPA to shift pixel values synchronously with a scanning mirror (this process is referred to as time delay and integrate [TDI]) can significantly improve the sensitivity of scanning systems relative to those using conventional analog FPA technology. With N stages (e.g., N columns assuming a row-wise scan) of TDI, the total integration time increases by a factor of N relative to a single TDI stage, resulting in an SNR improvement of $\sqrt{N}$. Conventional FPA technology typically supports no more than ~16 stages of TDI. Lincoln Laboratory has developed a 250-megapixel LWIR sensor based on a simple one-dimensional scanner and a 256 × 256 format DFPA configured to support 256 stages of TDI. Figure 1 presents an example 250-megapixel aerial LWIR image of Boston, collected at a 0.25 Hz frame rate [10]. The sensor was packaged in a 26-inch gimbal weighing 205 lb and provided a proof-of-principle demonstration of DFPA technology. Second-generation airborne sensors, now in development, will utilize a single 640 × 480, 20 □m pitch DFPA to produce even larger-format, higher-resolution imagery.

On-Chip Filtering

DFPA operations consisting of (1) controllable integration time, (2) up and down counting, and (3) orthogonal transfer enable the compact, low-power implementation of both spatial and simple temporal filtering operations. On-chip filtering offers the potential for new imaging modalities and extremely low-SWaP sensor systems for image exploitation.

Real-Time Spatial Image Filtering

Spatial filtering involves the convolution of an image with a filter kernel. In the DFPA implementation of a spatial convolution, each element in a filter kernel **K** (a matrix with I rows and J columns) is interpreted as an instruction. Consider the $K_{i,j}$ element; the counter is configured to count up or down depending on the sign of the element, and the integration time is set to a value proportional to the scalar value of the matrix element. With the DFPA so configured, an image corresponding to the $K_{i,j}$ instruction is collected. The next kernel element, say $K_{i,j+1}$, is selected; the current digital image is then shifted according to the selected kernel element subscript (e.g., the digital image is shifted one column to the right in this example), and an image is collected per the value of the $K_{i,j+1}$ filter element. The final filtered image is read out after all the kernel operations have been executed. Examples of on-chip spatially filtered imagery are shown in Figure 7. By exploiting the ability to split the input register into two subregisters, the DFPA can simultaneously apply two filter kernels to the input image [5].

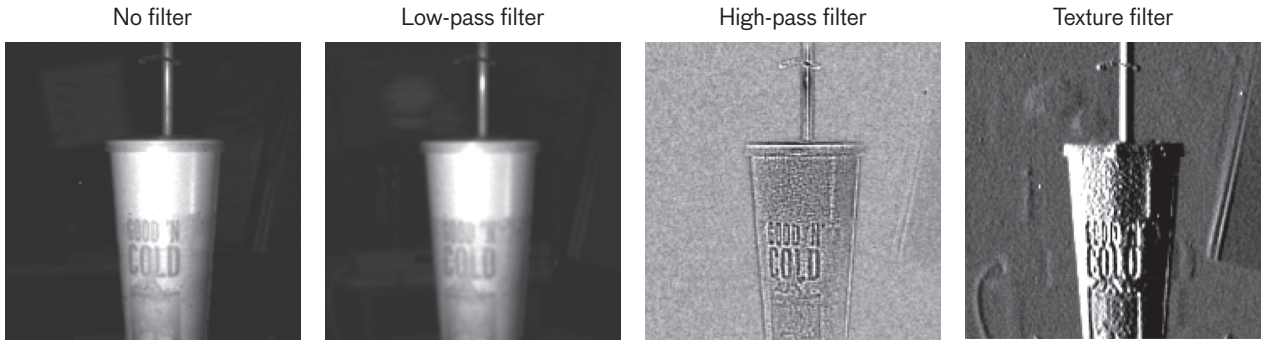

FIGURE 7. Utilization of the orthogonal digital data transfer function in coherence with the in-pixel compute function can result in a real-time two-dimensional convolution of the image with a predefined filter kernel. All of the filtered imagery above was processed as the image was collected rather than after image readout.

REAL-TIME TEMPORAL FILTERING

Temporal filtering based on differencing successive images can be easily implemented with the DFPA. The counter is programmed to first increment pulses and next, before image readout, decrement the incoming pulse train, and then read out the difference between the successively collected images. Only areas in the scene that have changing signal, caused by object motion or signal modulation, produce a signature in the resulting image.

As an example, fast temporal filtering enables the DFPA to detect the track of a bullet in flight by sequentially collecting many image differences prior to data readout. Figure 8 displays a shooter holding a pistol within a 50-foot range from the DFPA imager and a single raw image of the highlighted field of view showing a bullet fired at a speed of approximately 350 meters per second. The DFPA was programmed to collect 40 consecutive 200 μs integration periods prior to readout. The counter was configured to alternate between up and down counting intervals. After this 8 ms total integration time, the frame was read out, and the process was repeated. In this way, high-frequency events (e.g., a period <200 μs) can be captured while reading out at a rate 40 times slower than the high frequency of interest.

High-speed, in-pixel processing removes stationary clutter from the image while retaining the signal of interest (i.e., the bullet trajectory). Fast-moving objects, such as the bullet and the muzzle flash (hot gases escaping the gun barrel), produce white and black striped patterns; the in-pixel presence of the bullet while up counting and down counting results in alternating white and black stripes, respectively. Stationary and slowly moving objects, such as the gun barrel, are not detected. The in-pixel filtering allows "clean" imagery of the bullet trajectory to be read out at data rates between one and two orders of magnitude lower than what would be required using conventional imagers.

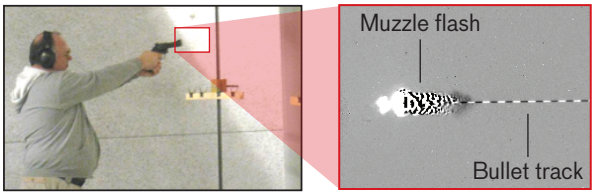

FIGURE 8. The DFPA successfully images a 350-meter-per-second bullet fired from a pistol within a 50-foot range. On-chip processing removes stationary and slowly moving objects, and displays high-velocity objects (e.g., the muzzle flash and bullet track) as striped patterns.

IMAGE-WIDE LOCK-IN AMPLIFICATION

Up and down counting can also be used to implement array-wide lock-in amplification, in which the image is effectively multiplied or mixed with an external frequency (e.g., local oscillator [LO]). Pixels in which the frequency is present (and in phase) will be detected. Multiple frequencies can be detected by sweeping the LO frequency and/or employing temporal compressive sensing techniques. For example, the digital pixel can implement compressive sensing using the random modulator preintegrator (RMPI) technique in which the input signal is modulated by a random control signal defined

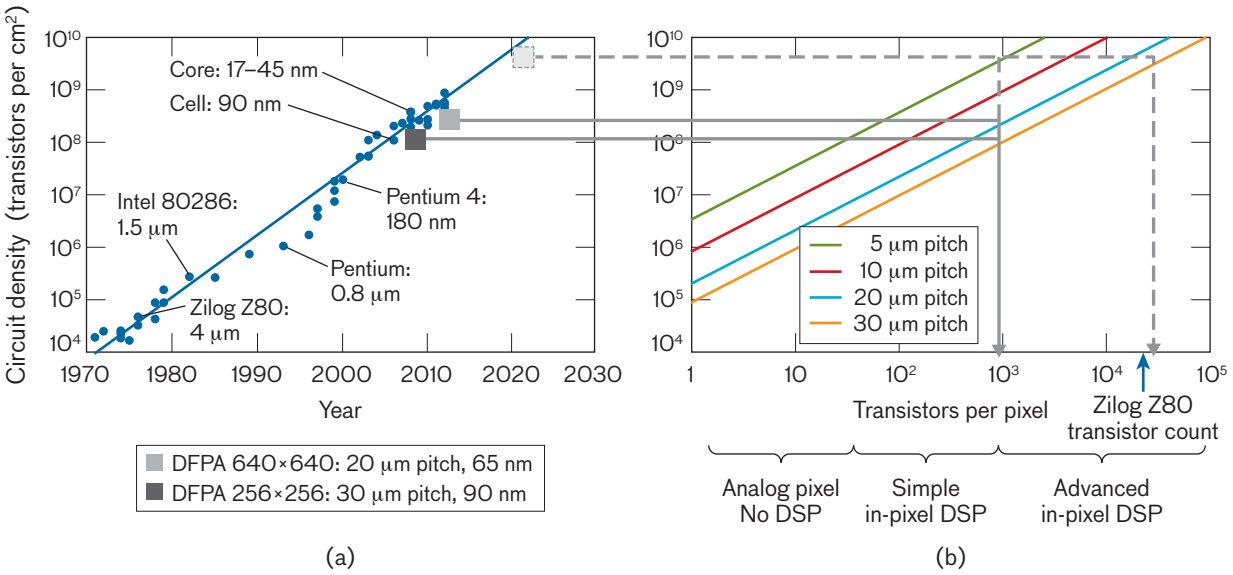

FIGURE 9. (a) The circuit transistor density and trend line for state-of-the-art commercial microprocessors plotted versus the year each microprocessor was introduced to the marketplace [13]. (b) The maximum number of transistors that can be packed into a pixel unit cell as a function of the circuit transistor density for several pixel sizes between 5 to 30 □m. A magnitude estimate of the number of transistors required to achieve three levels of digital processing within the unit cell is also indicated. By leveraging deeply scaled CMOS processes, DFPA technology enables designers to miniaturize pixel pitch and/or increase on-chip processing capability depending on application-specific needs.

by a random sequence of +1 and −1 amplitudes (implemented by a random sequence of up-down count commands) with the resultant modulated signal accumulated by the in-pixel counter [11]. The recent development of a multifunction pixel whereby the 16-bit, in-pixel counter can be configured as two independently controlled 8-bit counters allows in-pixel detection of a single frequency at two phases, thus enabling phase-independent frequency detection (e.g., in-pixel, in-phase, and quadrature detection). In addition, the multifunction pixel can be configured to simultaneously collect a conventional 8-bit image while also performing, for example, 8-bit lock-in amplification [12].

Future Directions

The transition of DFPA technology to the industrial base must be addressed as the technology matures. One approach to technology transition is the development of DFPA component libraries; individual components (e.g., I-to-F converter, DFPA counter/register) can be packaged into self-contained modules in a manner analogous to those used for conventional digital circuits (e.g., flip-flops). DROIC designers can then employ the basic components into their own (i.e., proprietary) application-specific designs.

Efforts to apply DFPA technology to shorter wavelengths (e.g., shortwave and midwave infrared wavebands) will require reducing unit-cell pitch.[3] To maintain or increase the unit cell's dynamic range will require employing increasingly deeply scaled, higher-density complementary metal-oxide semiconductor (CMOS) processes (e.g., 65 nm or 32 nm CMOS fabrication processes). In addition, photon flux typically decreases with decreasing wavelength, necessitating an increase in the in-pixel conversion gain, or, equivalently, a reduction in the number of photoelectrons per digital count. Lincoln Laboratory is actively pursuing techniques to increase the in-pixel conversion gain.

3. Nyquist spatial sampling requires pixel pitch ≤0.5 λ_{cutoff} f/# where λ_{cutoff} and f/# are the cutoff wavelength and f-number, respectively. As pitch is proportional to the wavelength, shorter wavelengths require smaller pitch pixels for fixed f/# optics.

Higher-density CMOS fabrication processes can also be used to increase in-unit cell processing capacity; the extrapolated unit-cell transistor count, shown in Figure 9, suggests the feasibility of advanced in-pixel signal processing in smaller pixels within the next decade. Sophisticated in-unit cell processing, coupled with inter-pixel data communication and control structures, would enable massively parallel computational imagers and resultant sensor systems with capabilities far beyond what are achievable today. ■

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APPENDIX A

Example Infrared Scenario and Calculation

Figure A.1 illustrates a sensor that has a thin lens of diameter D imaging a scene of radiance L onto a detector array located at the back focal distance of the lens. For simplicity, assume that the background (located in the far field of the lens) can be represented as a perfectly efficient blackbody emitter at a fixed uniform temperature and that the atmospheric radiance and transmittance can be ignored. In this case, the total received photoelectrons per pixel N_e can be approximated by the following expression:

$$N_e = \frac{\pi L_B \eta_{Optics} \eta_{DE} A_{Det} t}{4\left(f/\#\right)^2} \quad \text{[electrons]},$$

where

L_B = Blackbody radiance (in-band photons/cm^2/sr/s)
η_{Optics} = Optical transmission
η_{DE} = Detection efficiency
$f/\#$ = "F-number" (focal length/aperture diameter)
A_{Det} = Detector area (cm^2)
t = Integration time (s)

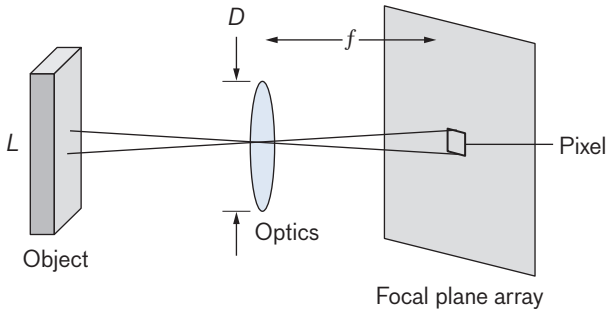

FIGURE A.1. A simplified optical sensor.

The in-band blackbody radiance is given by

$$L_B = \int_{\lambda_{Cut\text{-}on}}^{\lambda_{Cut\text{-}off}} \frac{2c}{\lambda^4\left(e^{c_2/\lambda T} - 1\right)} d\lambda \quad \text{[photons/cm}^2\text{/sr/s]}$$

where

$\lambda_{Cut\text{-}on}$ = Cut-on wavelength (μm)
$\lambda_{Cut\text{-}off}$ = Cut-off wavelength (μm)
c = Speed of light (m/s)
T = Background temperature (K)
c_2 = Second radiation constant (1.438769 cm K)

Assuming a background temperature of 310 K, a focal length of 22 mm, f/2 optics, a detector pitch of 30 μm, $\eta_{Optics} = \eta_{DE} = 1$, a waveband of 9 μm to 11 μm, and an integration time of 1 ms, we get a total background signal equal to ~200 million photoelectrons (as shown in Figure 5).

APPENDIX B

DFPA Noise Characterization

An expression for the total integrated root-mean-square (rms) noise electrons n_e after the digital register has accumulated N_{Trigger} counts is provided in the equation below [4, 5]

$$n_e = \frac{CV}{q}\sqrt{\frac{N_q}{12} + \frac{4kTt_{\text{Int}}}{C^2V^2R_d} + \frac{N_{\text{Trigger}}q}{CV} + \frac{N_{\text{Trigger}}kT}{CV^2} + \left(N_{\text{Trigger}}^2\left(\alpha_D^2 + \alpha_{\text{DROIC}}^2\right) + \left(\frac{e_n}{R_d}\frac{t_{\text{Int}}}{CV}\right)^2\right)\left(ln\left(\frac{t_{\text{Meas}}}{t_{\text{Int}}}\right)\right)}$$

[electrons]

Symbol	Definition	Nominal Value
t_{Int}	Integration time (s)	Variable
C	Capacitance (fF)	~1–2.5
V	Count trigger voltage (V)	Variable 0.2–0.5
q	Electronic charge unit (C)	1.6×10^{-19}
k	Boltzmann's constant (JK^{-1})	1.38×10^{-23}
T	DFPA device temperature (K)	68–85
α_{ROIC}	ROIC gain noise 1/f alpha coefficient	Order [10^{-5}]
α_D	Detector 1/f alpha coefficient	Order [10^{-5}]
t_{Read}	Readout time (s)	Variable
t_{Meas}	Total measurement time (s)	Variable (t_{read} + t_{Int}) × number of frames used in measurement
e_n	Transistor noise voltage @1 Hz ($V/\sqrt{Hz}$)	2.2×10^{-5} (IBM design manual 90 nm process node)
R_d	Detector resistance (mega-ohms)	~150 (varies with detector material)
N_{Trigger}	Number of counter triggers in t_{Int}	Varies with input current
N_q	Quantization constant	2 or 1
LSB	Least significant bit or total number of photoelectrons per digital count (electrons)	~1200–8000

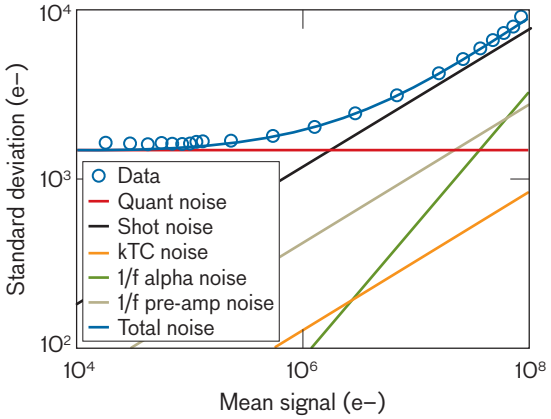

FIGURE B.1. Plot of DFPA noise model with measured data. Here the measured input current was 4 nA, V = 0.53 V, corresponding to an LSB = 3576 photoelectrons/digital count, N_q = 2, $\alpha_D + \alpha_{ROIC} = 2.2 \times 10^{-5}$, T_{Read} = 423 μs, and R_d = 150 mega-ohms. To compute measurement noise statistics, 128 frames were used. $\alpha_D + \alpha_{ROIC}$ were model-free parameters.

The net rms noise represents the root sum square of four independent noise terms. The first term represents the quantization noise and corresponds to the unknown charge on the integrating capacitor after the camera shutter is closed; the value N_q can take on values of 1 or 2 depending on whether the charge on the integrating capacitor is discharged prior to opening the shutter or not, respectively. The second term represents the Johnson or thermal noise generated by the detector resistance; the third term represents the noise associated with resetting the integrating capacitor; and the fourth term represents the slowly varying 1/f noise associated with both the detector and the DROIC analog front-end components [5]. The above model has been validated with measured data, as shown in Figure B.1.

About the Authors

Kenneth I. Schultz is an assistant leader of the Active Optical Systems Group at Lincoln Laboratory. Since starting at the Laboratory in 1987, he has worked primarily in the development and exploitation of passive and active electro-optic sensors. From 1991 to 1993, he served as chairman of the laser radar/lidar session of the International Conference on Lasers and Applications. He received the chairman's award for the Atmospheric and Midcourse Discrimination Technology session of the 1994 American Institute of Aeronautics and Astronautics/Ballistic Missile Defense Organization (AIAA/BMDO) Interceptor Technology Conference and received the best paper award at the 2001 AIAA/BMDO Technology Conference. For his work on ground-based laser measurements of satellite vibrations, he received the Naval Research Laboratory Review and Berman Awards. In 2010, his team accepted an R&D 100 Award for the digital-pixel focal plane array technology. He holds a bachelor's degree from the Massachusetts Institute of Technology and master's and doctoral degrees from the University of Pennsylvania, all in electrical engineering.

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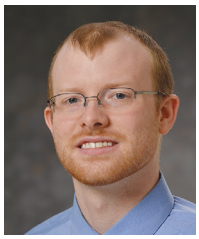

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