An Active Filter Achieving 43.6dBm OIP₃
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Abstract — An active filter with a 50 Ω buffer suitable as an anti-alias filter to drive a highly linear ADC is implemented in 0.13 μm SiGe BiCMOS. This 6th-order Chebyshev filter has a 3 dB cutoff frequency of 28.3 MHz and achieves 36.5 dBm OIP₃. Nonlinear digital equalization further improves OIP₃ to 43.6 dBm. Measurements show 92 dB of rejection at the stopband and a gain of 49 dB. The measured in-band OIP₃ of 43.6 dBm is 19 dB higher than previously published designs.

Index Terms — Active filter, anti-alias filter, analog-to-digital converter, OIP₃, nonlinear digital equalization, spur free dynamic range (SFDR).

I. INTRODUCTION

A receiver with high spur free dynamic range (SFDR) increases the ability to detect small signals in the presence of large ones by preventing distortions that mask low-power emitters. A wireless receiver with high SFDR demands a linear analog-to-digital converter (ADC). Often the ADC designers focus mainly on the ADC linearity, assuming the input to the ADC is perfectly ideal. In practice, however, the receiver is only as strong as the weakest link in the chain, and without careful design, the anti-alias filter and ADC driver can be the weak link. For instance, a 16-bit ADC can have 90 dB or higher SFDR only if the input has an SFDR of at least 90 dB. If the desired signal level at the input to the ADC for maximum signal-to-noise ratio (SNR) is 0 dBm, the cascaded third intercept point (IP₃) of the filter and the ADC driver at its output must be made higher than 45 dBm to achieve this specification. The goal of our work is to implement such a highly linear anti-alias filter with 30 MHz bandwidth and 90 dB stopband rejection.

The anti-alias filter is typically a large LC filter. A surface acoustic wave (SAW) filter is an alternative to the lumped LC filter with a much smaller footprint, but a SAW filter with over 20 MHz bandwidth and 90 dB stopband rejection induces significant loss (over 20 dB), requiring the ADC driver to supplement the gain. Neither an LC nor a SAW filter is an integrated on-chip solution, which has the added benefit of a reduction in receiver power dissipation by eliminating the power hungry 50 Ω buffer.

A filter integrated into a Si IC is typically an active filter such as op-amp-based RC or gmC. The switched capacitor filter is excluded because of its discrete operation in time, thus requiring anti-alias filtering in a subsequent stage. [1] demonstrated an in-band output IP₃ (OIP₃) of 19.5 dBm using an op-amp-based RC filter. [2] and [3] demonstrated 24 and 18.5 dBm for gmC filter with a degenerated gm stage and with an active inductor load, respectively. However, all fall short of the required 44 dBm output IP₃. The requirement to implement a 50 Ω buffer to drive the off-chip ADC further complicates the achievement of high linearity. We have implemented a highly linear active filter with a 50 Ω buffer, making a fully integrated receiver chip with high SFDR feasible.

II. DESIGN

We have selected an op amp-based RC configuration to potentially achieve the highest linearity for the low-pass filter [4]. The required stopband rejection is 90 dB. A 30 MHz passband requires 9th-order Chebyshev type if the stopband frequency is 60 MHz. If instead the ADC is oversampled by 6x, then a 5th-order filter meets the stopband rejection at 180 MHz. High linearity for the filter is achievable only with a large loop gain and unity-gain bandwidth of the op-amp. The unity-gain bandwidth required for the op-amp in the 5th-order filter is > 18 GHz. In order to reduce the op-amp unity-gain bandwidth requirement, the filter is instead configured as 3 stages of 2nd-order filters with a gain stage inserted between filter stages to minimize loading. Fig. 1 shows a block diagram of the gain and filter stages and a 50 Ω buffer for testing. Each stage has a dc offset correction circuit and a bandgap referenced bias circuit supplying bias currents to all the circuit stages.

Fig. 1. A block diagram of filter/gain stages with 50 Ω buffer.
Fig. 2 is a schematic of the op-amp used in the gain/filter stages. Once the open loop gain of the op-amp is above 30 dB, its PMOS active load limits the linearity. Thus, a resistor load, $R_L$, is used instead. The MOS resistor operating in triode region is not used to avoid additional nonlinear components. The dc bias current of 1 mA for the differential pair $B_1$ and $B_2$ was selected to meet both the acceptable noise and linearity parameters. For instance, the input noise spectral density is designed to be $\sim 7 \text{nV/}\sqrt{\text{Hz}}$ for the overall filter stage. The sufficient open loop gain of $\sim 40$ dB and a high dominant pole of $\sim 200$ MHz at the collector load ensure linearity.

In order to test the filter and drive an off-chip 16-bit ADC at high sampling rate, a 50 $\Omega$ buffer driving $1 \text{V}_{\text{pp}}$ with $> 90$ dB SFDR is necessary. This 50 $\Omega$ buffer can further degrade the output linearity. We modified the feedforward amplifier proposed in [5] to 50 $\Omega$ buffer with a reduced propagation delay in the error correction path. The cascaded error correction pair extends the bandwidth from 31 GHz to 62 GHz and improves the OIP$_3$ by 2 dB. The 50 $\Omega$ buffer itself achieves a 40-dBm OIP$_3$.

### III. Measurement Result

The active filter with a dc offset correction and 50 $\Omega$ buffer is implemented in 0.13 $\mu$m SiGe BiCMOS. The IC was directly wire-bonded to a PCB. Fig. 4 is a photo of the IC.

Fig. 4. Die photograph of the active filter with 50 $\Omega$ buffer.

The cascaded filter, gain stages, and 50 $\Omega$ buffer have a gain of 49 dB and a 3 dB cutoff frequency of 28.3 MHz, and 92 dB rejection at 180 MHz as shown in the S-parameter measurement performed with a network analyzer (see Fig. 5). The network analyzer has a lower cutoff frequency of 10 MHz. Therefore, we used a spectrum analyzer and a signal generator to verify the low end cutoff frequency at 2.5 kHz.

![Simulated open loop response of gain and phase of the op-amp.](image)
To measure OIP3 we used several two tone measurements from 3 MHz to 40 MHz with the tone spacing from 0.08 MHz to 20 MHz. The median of measured OIP3 across the 124 two-tone stimuli is 36.5 dBm. Because the signal generator has a poor SFDR at frequencies below 100 MHz, the signal generator input frequency tones are set to > 950 MHz and a linear mixer is used to down-convert the two tones to frequencies within the 30 MHz filter band. Fig. 6 is a spectrum analyzer output of the two tones, with frequencies 7 MHz and 8 MHz and measured output power of -1.4 dBm and -1.6 dBm, showing > 75 dB SFDR.

To further improve the linearity, digital equalization is applied after the off-chip ADC. The nonlinear equalizer consists of the weighted sum of products of time-delayed values from the input stream to capture the memory effect in the harmonic and intermodulation terms. The delay, polynomial order and the number of terms were determined by applying a series of targeted frequency tones at the input of the filter and identifying the best polynomial using a constrained optimization procedure as in [6]. The equalizer was limited to three nonlinear terms, each term being a polynomial of up to 3rd order. As shown in Fig. 7, the implementation was limited to six multiplications and three additions per sample to minimize the power dissipation of the digital equalizer. The gate count is approximately 18,630 using 16-bit multipliers with truncation, and the simulated power dissipation is 2.7 mW. The filter drives a 16-bit ADC sampled at 180 MHz (a 16-bit ADC with 208 MSPS was not available at the time of testing), and a logic analyzer captures the digital output. The digital compensation algorithm is applied to the digital output in a bit-true MATLAB simulation. Fig. 8 shows a histogram of the measured maximum distortion level (i.e., intermodulation and harmonics) as two tones and their frequency spacing were swept from 3 MHz to 40 MHz and 0.08 MHz to 20 MHz, respectively. The output power level of the two tones is 0 dBm each. The horizontal axis is the power level of the worst distortion component before (dark blue) and after (light blue) the compensation. The vertical axis is the occurrence of the distortion level. The compensated output shows the median distortion of -86.4 dBm after the compensation based on 124 tone sets. The median improvement is 14 dB, effectively improving OIP3 by 7 dB. Table 1 compares the performance of anti-alias filters in [1-3] with our work.
Opinions, interpretations, conclusions and recommendations are those of the authors and are not necessarily endorsed by the United States Government.

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REFERENCES


### TABLE I

<table>
<thead>
<tr>
<th>Reference</th>
<th>OIP3 (in-band)</th>
<th>3 dB Cutoff Frequency</th>
<th>Gain</th>
<th>Stopband Rejection</th>
<th>Input Referred Noise</th>
<th>Power</th>
<th>Technology</th>
</tr>
</thead>
<tbody>
<tr>
<td>[1]</td>
<td>19.5 dBm</td>
<td>1.92 MHz</td>
<td>8.5 dB</td>
<td>63 dB</td>
<td>46 μVrms (integrated)</td>
<td>11.6 mW</td>
<td>0.8 μm BiCMOS</td>
</tr>
<tr>
<td>[2]</td>
<td>24 dBm</td>
<td>1, 2.2 or 11 MHz</td>
<td>-6 dB</td>
<td>Not reported</td>
<td>5 nV/√Hz</td>
<td>55 mW</td>
<td>0.13 μm CMOS</td>
</tr>
<tr>
<td>[3] (low pass portion)</td>
<td>18.5 dBm</td>
<td>15 MHz</td>
<td>0 dB</td>
<td>60 dB</td>
<td>15.2 nV/√Hz Or 50 nV/√Hz for low power</td>
<td>184.8 mW</td>
<td>0.6 μm CMOS</td>
</tr>
<tr>
<td>This work</td>
<td>36.5 dBm</td>
<td>28.2</td>
<td>49 dB</td>
<td>92 dB</td>
<td>8.4 nV/√Hz</td>
<td>79 mW</td>
<td>0.13 μm SiGe BiCMOS</td>
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<tr>
<td>This work</td>
<td>43.6 dBm</td>
<td>28.2</td>
<td>49 dB</td>
<td>92 dB</td>
<td>8.4 nV/√Hz</td>
<td>81.7 mW</td>
<td>0.13 μm SiGe BiCMOS</td>
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