Lincoln Laboratory is developing fully Si CMOS–compatible technologies for GaN high-electron-mobility transistors (HEMTs) and circuits for RF applications. GaN-based HEMTs have demonstrated impressive capabilities in power density and voltage in laboratory devices. Transmit/receive modules using GaN HEMTs could yield more output power than GaAs-based modules. Measured $f_T$ and $f_{\text{max}}$ are in the 50 and 70 GHz range, respectively, for HEMTs with 120-nm nominal gate length.

**KEY FEATURES**

- Exploits processing tools to improve device performance, uniformity, and yield
- Reduces costs because of inexpensive Si substrate, large wafer size, and expected CMOS-like high yield
- Facilitates wafer-scale 3D integration of GaN with CMOS circuits to enhance functionalities with improved size, weight, and power benefits
Measured $f_T$ (a) and $f_{\text{max}}$ (b) of HEMTs from all 26 dies on a 200-mm-diameter wafer. The gate length is nominally 120 nm and the gate to source and drain spacings are 0.5 and 1.0 μm, respectively. The drain and gate biases are fixed at 10 V and –2.2 V, respectively. The median $f_T$ is 50 GHz and the highest is 57 GHz. The median $f_{\text{max}}$ is 78 GHz, with 80 GHz as the highest. The standard deviation is 2.9 GHz for both. The drive current and peak transconductance are also very uniform, with approximately 5% variation across the wafer.

Features of Lincoln Laboratory Process

- All the metallization is gold free and patterned by etching instead of liftoff to be fully CMOS compatible.
- High-performance HEMTs show the maximum drive current of 1 mA/mm and the peak transconductance exceeding 400 mS/mm.
- The breakdown voltage is approximately 90 V with 1 μm gate to drain spacing.
- The overhang of the T-shaped gate serves as the field plate instead of using an added metal layer for this function.
- Good processing control enabled the fabrication of the HEMT showing a tight distribution of $f_T$ and $f_{\text{max}}$ values. Such high yield and good uniformity is essential for delivering low-cost large-size GaN circuits.

Going Forward

- Process wafer thinning with backside vias
- Develop wafer-scale 3D integration with CMOS wafers
- Continue refining the GaN growth technique and optimizing the layer structures for HEMTs
- Add more metal layers and passive components for GaN monolithic microwave integrated circuits

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